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Built-in Performance Characterization of Embedded Mixed-Signal Circuits

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Built-in Performance Characterization of Embedded Mixed-Signal Circuits

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Dedicated to my wife and parents

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Built-in Performance Characterization of Embedded Mixed-Signal Circuits

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Recent advances in semiconductor technologies enable the integration of previously disparate designs into a single system-on-chip (SOC). While the SOC offers significant benefits in reducing overall design cost, it poses significant challenges for testing. A traditional specification-based test method is no longer attractive in testing deeply embedded analog and mixed-signal circuits due to limited I/O accessibility, limited tester resources and signal integrity issues. Built-in Self-Test (BIST) has been considered as a promising solution to overcome such difficulties; however its widespread adoption has been hindered for several reasons.

The aim of this thesis is to develop efficient self-test techniques for embedded analog and mixed-signal circuits, which provide test accuracy equivalent to a traditional specification-based test, but with minimal overhead in

terms of performance, area and additional test cost associated with DFT circuits. The outcome of the self-test is a set of performance parameters, allowing us to evaluate DUTs with respect to its specification, and to guide a self-repair mechanism efficiently. A compact representation of analog signals and its simple recovery algorithm are developed to replace a traditional analog signal test. With this alternative representation, the hardware overhead associated with analog signal generation and measurement is significantly reduced, thereby the requirements for BIST implementation are substantially relaxed. To overcome accuracy and precision limitations posed by on-chip designs for test or existing hardware used for test, a spectral prediction technique and a statistical digital equalization technique are studied. These techniques are incorporated into a loopback test scheme where analog cores can be tested with pure digital methodologies, but where test accuracy is yet considerably limited due to fault masking problem and precision limitation. An efficient fault diagnosis technique based on the BIST techniques and circuits for self-repair, is also investigated. This study constitutes the first attempt at the diagnosis of analog faults which accounts for existing BIST and self-repair circuits.

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Chapter 1

Introduction

1.1 Motivation

The fundamental difference between analog testing and digital testing is that analog testing handles continuous signals, whose value has, in nature, infinite precision rather than two states like either zero or one. This makes analog signal stimulation and measurement procedures very complicated. For example, analog comparators and digital comparators (Exclusive-or gate) perform a similar function which compares two values and generates one of two states depending on the outcome of the comparison. Testing of digital comparators involve applying four different patterns and comparing the outcomes with expected values. However, in addition to this basic functional check, testing of analog comparators needs to measure the minimum magnitude difference (resolution) of two analog inputs for which the comparators work correctly. In this scenario, the search space for potential analog inputs may be infinite, making test input generation extremely challenging. Moreover, for a comparator of higher resolution, the outcome may be more sensitive to the accuracy of test inputs. When uncertainty level of the test input exceeds the resolution of the comparator due to random and systematic errors, the outcome would likely be erroneous, and leads to misinterpretation of test results.

In addition to resolution parameter above, the performance of an analog comparator, which is one of the simplest designs of mixed-signal circuits, is often described by many parameters such as noise, offset, Common-Mode Rejection Ratio (CMRR), response time, delay, swings, impedance and so on. Traditionally, analog and mixed-signal testing rely on measurement of these design specifications. The measured parameters are compared against tolerance limits of specifications to make sure that the device can perform the described operation. Testing these parameters is quite time-consuming as different parameters, generally, require different test setups and thus the test procedure is essentially sequential.

Accurate and safe transfer of analog signals to external measurement equipment poses an additional problem compared to digital signals. A Device Interface Board (DIB) provides interface between a DUT and test equipment. DUTs that are purely digital typically require a simple DIB that simply provides connectivity between the DUT and the test equipment. For analog and mixed-signal DUTs, much more elaborate DIBs are required, which contain various active and passive elements. In order to identify true defects in the DUT, it is important to be able to distinguish between a failure of a device and a failure caused by the data transfer channel through the DIBs.

1.1.1 Embedded Analog Core Test

The integration of previously disparate semiconductor technologies in System-On-Chip (SOC) or System-In-Package (SIP) designs poses significant

challenges for testing of the embedded analog and mixed-signal cores [53]. A conventional core-level test may not be attractive for several reasons. Due to the limitation on the number of analog ports, the access to individual cores is realized with analog switches or muxes, which were not necessary in testing a discrete design. The insertion of such test access points always has an impact on overall system performance and area. In addition, the issues associated with accurate transfer of analog signals become more severe as frequent switching of analog signals may contaminate the analog response. It may cause an increase in test cost due to the overhead of initialization and settling time. Limited resources in Automatic Test Equipment (ATE) is another factor which increases overall test cost [53].

In order to overcome such obstacles, some tester functions have begun to be implemented with specially designed on-chip circuits, or replaced with existing digital or analog circuits. Significant test cost can be reduced by implementing such self-testing analog cores. The potential problem with this approach is that the design and test cost associated with complete on-chip implementation of a traditional analog test setup may be unacceptably expensive.

As an alternative to the traditional test setup, a signature-based test has been introduced [5, 11, 29, 49, 58, 62, 81]. In a signature-based test, the performance of analog cores is indirectly measured with a specially crafted test input [11, 29], special DFT circuits [81], or by reconfiguring DUTs favorable for testing [5, 58]. The major goal of these alternative approaches is to alleviate

overhead for complicated test input generation and data acquisition. On the other hand, when a mixed-signal system includes both digital processing units and data conversion units, a traditional test set-up can be readily realized with these units. Digital to Analog Converters (DACs) and Analog to Digital Converters (ADCs) constitute a pair to generate and capture analog signals respectively. This test scheme, commonly known as a loopback test scheme, enables efficient testing with traditional digital methodologies as it eliminates the need for additional analog stimuli and measurement.

However, the widespread adoption of these approaches has been restrained due to several reasons. First, in signature-based testing, the signature may have strong correlations with faults in DUTs and can be successfully applied to detect the faults; however, the performance information in a specification sheet may be lacking. The evaluation of DUTs with specification is important as the performance information is often used in other manufacturing phases such as calibration and diagnosis. In addition, an extensive simulation is required to determine the limits of acceptable signature values, which is not usually required in a traditional test and design. Therefore, in order to avoid this redundant design and test cost, and utilize the test result to improve yield in other manufacturing phases, the signature which contains performance information of DUTs and the algorithm which can translate this correlation, are essential.

Secondly, most studies on these approaches assume that existing hardware or special designs used for test are ideal [50, 54, 55]. However, many

subtle interactions with DFT circuits or existing hardware used for test make the measured test response behave differently from the actual performance of the DUT. For example, in the loopback-based test scheme, two signal paths which contain the DAC and the ADC respectively, are reconfigured into one signal path, and the overall response of the cascaded signal path is then measured. Unfortunately, this test scheme may not be sufficient to guarantee the performance of individual signal path due to potential fault masking. The fault masking may occur when one of the signal paths is overqualified in the presence of a fault in another signal path, leading to the overall performance of the loopback path to be completely fault-free. Therefore the loopback response does not directly represent the functional specifications of individual blocks or paths under test. The pass/fail decision based on the pure loopback test may lead to serious yield loss and test escape.

Testing static linearity errors of data converters may cause more serious fault masking problems. While the aforementioned fault masking problem makes the faults of the analog circuits under test undistinguishable, the linearity error interaction tends to cancel, making the faults unobservable. For example, if the transfer function of the DAC in loopback mode is the perfect inverse function of the ADC, the data collected from the loopback response will be fault free regardless of the degree of the non-linearities of the DAC and the ADC.

Thirdly, whereas a traditional test using external measurement utilizes several techniques to ensure high precision of analog signals, these approaches

may suffer from low test accuracy due to difficulties in on-chip implementation of such DFT techniques. As the performance of a device continue to improve, it may be increasingly difficult to achieve highly accurate on-chip test setups. This problem is somewhat related to the second issue as the precision limitation may also make the fault invisible. For example, consider the ADC whose static linearity is tested with analog signals generated from the DAC on the same die, and the linearity information of the DAC is provided. There is no straightforward way to compensate for this linearity error and prevent it from contaminating the test response, unless the resolution of the DAC far exceeds the ADC under test. Therefore, the finite resolution limits the achievable test accuracy, although the ADC and the DAC work correctly within the desired specifications. The issue can be extended to the situation where DUTs are tested with a low cost tester whose specification does not exceed the requirements.

1.1.2 Analog Fault Diagnosis

In general, faults in analog circuits can be classified into two categories: catastrophic and parametric faults [32]. Catastrophic or hard faults result in a complete failure of a desired circuit function. Most common catastrophic faults are opens and shorts. Parametric or soft faults are typically variations in process parameters which cause a circuit parameter value to deviate from its nominal value, resulting in failure to meet tolerance limits of the desired specifications by a small amount. As device dimensions are shrinking, the

yield loss due to parametric variations is rapidly increasing. Therefore rapid and accurate identification of weak spots in a design and potential problems in the manufacturing process is of significant importance to improve yield and reduce time-to-market [67]. This procedure is commonly known as fault diagnosis. In addition to the fundamental role of fault diagnosis, especially in analog circuits, fault diagnosis has gained considerable attention as a solution to guide self-repair mechanisms. The diagnosis process detects a fault and isolates the core or element associated with the fault, and finally a DUT is able to adapt itself to meet the required specifications.

In general, during the analog fault diagnosis, the effective values of the circuit parameters are determined by solving a set of equations, whose independent variables are obtained from measurements performed on a set of selected test points. The selection of suitable measurements is intended to highlight the presence of fault, so that the isolation of a faulty parameter is readily achievable. Depending on the types of circuits and approximation assumption, the equation can be either linear [2, 67, 78], or nonlinear [18, 19].

The problem with this approach, regardless of linear and nonlinear models, is that it assumes the availability of expensive external equipment for accurate and sufficient measurements [2, 16, 18, 19, 67, 76, 78]. The broad range of off-chip measurements may result in long diagnosis times since it involves, in general, different measurement setup and test stimuli. As the complexity of the analog systems increases, the fault diagnosis task become a bottleneck in delivering products to market in time.

1.2 Contribution

The major contributions of this thesis are the study and analysis of efficient self-test techniques for embedded analog and mixed-signal circuits in SOCs, which are summarized as follows.

- A conventional ATE-oriented specification measurement is replaced with an indirect low-cost measurement which utilizes an alternative compact analog signal representation.
- The fault masking problem is understood, and resolved to some extent with analog modeling and spectral analysis. This approach is validated through hardware measurement.
- The precision limitations posed by DFT or BIST circuits are alleviated with an equalization technique based on probabilistic analysis for test input.
- The application of DFT and BIST circuits is extended to analog fault diagnosis collaborating with circuits for self-repair.

The major drawbacks in a conventional ATE-oriented specification test and some previous research on a naive on-chip implementation of some ATE functions [9, 46, 57] are hardware cost to ensure accurate signal generation and acquisition. The alternative analog signal representation studied in this thesis significantly simplifies the signal acquisition and generation process. Unlike

a conventional analog signal representation with sampled amplitude information, analog signals are represented with much fewer number of time-domain parameters. Hence, the acquisition of those parameters can be performed with simple comparators and digital circuits. Also, as opposed to other research results which mostly focus on the detection of a fault [49, 62], the test response can be readily interpreted into performance parameters in a specification sheet, thereby allowing DUTs to be evaluated by comparing the measured performance directly against the specifications.

The fault masking and precision limitation problem are studied with the example of a loopback-based test scheme. A loopback-based test scheme has been extensively studied in many research, however the fault masking and precision limitation have retarded its widespread adoption. Firstly, to overcome the fault masking problem, the performance of each signal paths in a loopback mode is estimated individually, and thus we can avoid the errors which result from subtle interplay between two signal paths. The precision limitations is improved with a calibrated test input which accounts for the nonlinearity of the DAC. Based on the fact that the analog test input is applied several times due to the repeatability issue, the deterministic test input is treated as a probabilistic signal. By manipulating the weight factors of the probabilistic signal, the ADC is tested with highly linear analog signals where the DAC-induced nonlinearity is removed. This concept can be readily extended to a low-cost tester approach. Here a test input is calibrated considering the finite resolution of the tester.

Based on these self-test techniques, the analog fault diagnosis procedure is significantly facilitated. Most previous research relies on expensive and time-consuming measurement of several observation points to ensure accurate diagnosis [2, 16, 76]. Instead, the fault diagnosis procedure studied in this thesis uses the signature values to diagnose the fault in DUTs, thereby gaining a significant cost reduction associated with the measurement.

1.3 Approach Overview

This section presents a brief overview of approaches explored in this thesis. In order to reduce test cost associated with analog signal acquisition and excitation, a time-encoded signature based on a time encoding technique [42] is studied. The time encoding technique is the time domain representation of an analog signal as a discrete sequence of strictly increasing times. It has been widely studied in neuroscience to represent sensory information [41, 77]. While the classical time encoding technique aims at the perfect reconstruction of arbitrary analog signals, the time-encoded signature is designed for extracting minimum features from the test response of DUTs for a known input, thus the analog test response can be represented with much smaller parameters than the classical time encoding technique. The potential problem with the time-encoded signature is lack of a standard analysis method to understand the performance of DUTs from the signature. An efficient decoding algorithm based on a statistical approach is developed for this purpose. The decoding algorithm exploits the statistical correlation between the obtained signature

and the performance parameters of interest, and this correlation is modeled with a non-linear regression technique. The encoding mechanism studied in this thesis provides efficient means of capturing analog signals with simple analog comparators and digital circuits, and therefore a significant reduction in hardware overhead can be achieved when it is applied in BIST environments.

For analog systems which include data-converter units, analog signal acquisition and generation may be readily achieved. However, due to the fault masking problem, the accuracy of this approach cannot provide sufficient means guaranteeing the performance of DUTs. As a first step, the impact of the fault masking problem of dynamic parameter testing is studied mathematically with the example of two non-linear and noisy cascaded analog circuits. The study shows that it is very difficult to avoid the fault masking problem with a traditional approach due to the additive property of analog signals. A spectral prediction technique aims at attacking these challenges. A two-tone test input is applied to a DUT in loopback mode, and an off-chip analog filter and analog adder placed on Device Interface Board (DIB) produce a composite loopback response which can be decomposed into loopback responses of different weights. *Characteristic parameters* are obtained from their spectral representations, and are used as predictors for mapping equations based on statistical modeling of analog signal paths. This approach allows us to evaluate the dynamic performance of individual signal path, thereby the fault masking is significantly reduced.

The fault masking problem on the static parameter testing of the data

converters is also investigated. The study shows that the subtractive and additive property of the static parameters make the fault masking even more intricate. These properties make a sequential test approach [71] impractical, where one of the devices is tested separately and the loopback response is post-processed with the identified errors. A efficient digital equalization algorithm is developed to overcome such limitations. The transfer function of the DAC is estimated based on the obtained characteristic parameters from the spectral prediction technique and Chebyshev polynomials, and then the loopback test re-run with a calibrated test input which accounts for the non-linearity error of the DAC. The basic principle of Chebyshev polynomials is based on the idea that the transfer function of nth-order polynomials, can be accurately estimated by the weighted sum of Chebyshev polynomials whose coefficients are harmonic coefficients of a single tone response. The accuracy of a classical calibration technique which, in general, subtracts or adds digital bits to compensate the linearity error, depends on the precision of the devices. This thesis shows that this approach cannot provide accurate compensation for the error less than 1 LSB (LSB is a precision parameter). The equalization technique introduced in this thesis aims at achieving more accurate test accuracy by compensating the error less than 1 LSB. The equalization technique focuses on the linearization of a test input for a specific test setup, rather than a functional input in a normal mode. Weight factors are given to each code of the DAC, and by adjusting the weight factors, the cumulative probability of the analog input to the ADC is linearized. The major advantage of this

test approach is that the entire test including the equalization process, are performed in a pure digital domain.

Analog fault diagnosis methodology which collaborates with DFT circuits and circuits for a self-repair, is studied. This research suggests that various circuit designs used for its own purpose (test, calibration, and diagnosis) may cooperate to improve the overall efficiency. Existing fault diagnosis methods [2, 16, 18, 19, 67, 76, 78] reply on measurements of several test points, which usually involve external expensive measurements with different test setups and long ATPG time. Instead, in this thesis, information (signatures) provided by the BIST scheme is utilized, thereby reducing the overhead associated with the measurements. However, the accuracy and diversity of measurement obtained from the BIST is inherently inferior to external measurement. Imperfect signatures are compensated in two ways. Supplemented signatures obtained from re-configured DUT by parameter tuning overcome the diversity problem. Secondly, diagnosis accuracy is significantly improved by using an ensemble method, which has been widely used in data mining [51].

Chapter 2

Review of Analog and Mixed-Signal Test

This section provides a brief overview of some existing methodologies for analog and mixed-signal testing. The intent here is to highlight some of the difficulties associated with each of the methods in order to motivate the new methods described later. It should be noted however that many of these methods have met with considerable success in a variety of applications.

2.1 Standard Analog and Mixed-signal Test

A typical way to test analog and mixed-signal circuits is to measure the performance parameters in a device data sheet or specification sheet. The performance parameters may include electrical characteristics, timing of operation and absolute maximum ratings. The performance parameters listed in a specification sheet depends on the application intended by the design. In certain designs, AC parameters are the primary focus of the specification sheet, while they can be ignored or replaced with DC tests in other designs. However, in general, analog circuits are characterized by many kinds of AC, DC, parametric, frequency and transient parameters, and in addition, various operating conditions may produce infinite number of specifications. Thus,

one important task of test engineers is to develop optimal test procedures to optimize both test coverage and test time.

DC test involves the measurement of electrical characteristics such as power supply currents, leakage currents, impedance, power supply sensitivity, and performance characteristics such as DC gain, offset and transfer function. A common way to measure these DC parameters is to apply DC voltage or current, and then to measure the output response using a voltage or a current meter. Depending on the test parameters, the applied test input, measurement point, and test configuration may vary. For example, the measurement of open-loop gain and closed-loop gain of operational amplifiers requires different configurations.

On the other hand, sine waves are commonly used in AC parameter testing as appropriate sine wave sources are readily available and it is relatively easy to establish the quality of the sine wave. Examples of AC parameters are gain, phase, distortion, signal rejection and noise. AC parameter testing is often referred to as dynamic testing. The dynamic specifications are important in high-speed applications such as digital communications, ultrasound imaging, instrumentation, and IF digitization. Figure 2.1 shows the sine wave test setup. A sine wave generator provides the test signal while a clock generator provides a clock signal. By combining the output of a number of sine wave generators, test signals with multiple frequencies can be produced. For more flexible generation of test inputs, the test signal can be generated digitally and then converted to analog by using DACs. Long test time and complicated test

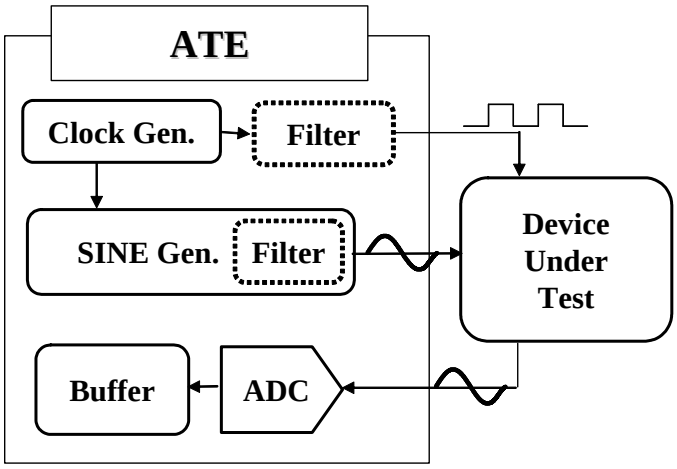


Figure 2.1: Typical Sine Wave Test Setup

setup for its application and measurement, make the AC parameter testing very expensive.

For a complex mixed-signal IC which includes digital circuits and analog circuits, it is tested separately for several reasons. The separation of digital and analog circuits provides easy access to each circuits and thus they can be characterized with a much more efficient fashion. In general, boundary cells are inserted between analog and digital blocks and enable direct access to these blocks. Test time is another reason for the separation. When the digital circuit is placed in the analog channel, the generation and measurement of digital test signals through analog blocks would be extremely inefficient. A similar separation technique is applied to provide easy access to individual analog blocks in a complex mixed-signal ICs. Analog switches or muxes are placed between individual analog blocks, and the test input and output are

transferred through analog test buses. The IEEE 1149.4 mixed-signal test bus standard is aimed at testing internal circuit nodes with minimal additional pin requirements, and chip-to-chip interconnect at the board level. The problem with this approach is that the separation always has a impact on the performance, and the test time for each block is additive, resulting in significant overall test times.

2.2 Related Work

As opposed to testing analog circuits with a typical test setup described above, there have been many studies to measure test specification values indirectly by using special test circuitry, existing digital or analog cores in a system, or specially crafted test inputs, and a combination of these methods. [5, 55, 59, 81] The major goal of these studies is to alleviate requirements for complicated test input generation and data acquisition, leading to a reduction in test cost involved in specification measurements.

Oscillation-based test has been proposed for this purpose [4, 5, 15, 31]. In oscillation-based test, a DUT is partitioned into several functional building blocks such as amplifiers, operational amplifiers, comparators, filters, voltage references and so on. During the test mode, each block is converted into an oscillator using some extra circuitry. The oscillation parameters of each block such as frequency and magnitude, are measured externally, and compared against predefined tolerance limits to determine whether the DUT is faulty or fault-free. The tolerance limits of the oscillation parameters is often de-

termined by Monte Carlo simulation, taking into account the variations of all important technology and design parameters. The oscillation architecture is chosen to maximize the sensitivity of the oscillation parameters with respect to the variations of the circuit parameters, thus the deviation of oscillation parameters is magnified in the presence of faults.

The major advantages of the oscillation-based test are a reduction in test complexity by eliminating test vector generation and a high compatibility with Built-in Self-Test. A comprehensive BIST scheme based on the oscillation-based test has been introduced in [62]. This scheme includes on-chip output analyzer which measures the oscillation parameters, and as a consequence, test excitation and acquisition can be performed purely on-chip. In this method, the responses of some internal nodes of a DUT in oscillation are also measured to increase fault coverage. However, the aforementioned oscillation test techniques have certain limitation that DUT is evaluated in oscillation parameter domain rather than in specification domain. As a consequence, test engineers should perform extensive simulations or measurements to determine the tolerance limits of the oscillation parameters, and in addition, it is difficult to use the test result in other manufacturing phases such as calibration and diagnosis.

To overcome such limitations, Predictive Oscillation Based Test (POST) has been introduced in [59]. In this method, in addition to the oscillation parameters described above, the sampled data of oscillation signals are used to predict the performance parameters of a DUT. A mapping function is derived

to relate the oscillation parameters and the performance parameters using adaptive regression techniques [25]. To extend its usage to the situation where the oscillation disappears due to excessive variations, Quasi-Oscillation Based Test (PQOBT) has been proposed [58]. In this method, a DUT is converted into a marginally unstable state. A pulse is applied as a test input, and the sampled data of a marginally oscillating DUT is used for predicting the performance parameters. This method, however, requires more complex and accurate data acquisition than previous approaches.

There have been several other studies focusing on the compact representation of output signal when a normal test input is applied [38, 81]. In these methods, the output response to a sinusoidal input is represented with three levels, positive, negative and zero; thus the output acquisition procedure is considerably simplified. This simplified representation is post-processed to quantify slope, symmetry and zero-crossing time of output signal. The simplified representation can be achieved using simple comparators, and its post-process can be performed in pure digital domain. Major advantages of this approach are that the performance parameters such as SNR and THD can be accurately extracted from this simple representation, and a high compatibility with BIST and a low-cost digital tester. This approach, however, may not be applicable when the phase of each harmonic components is different, as two harmonics of different phases are not synchronized and as a consequence the values of the post-processed parameters can be contaminated.

As an alternative to deterministic input signals, pseudo-random noise

is used as a test input [24, 54, 55, 70]. Unlike a sinusoidal signal which typically consist of a few fundamental frequencies, pseudo-random noise ideally includes infinite ranges of frequencies. By correlating statistical characteristics of output and input signals, transfer function can be constructed. While these approaches alleviate the test generation problem, it still requires a dedicated noise generator and its usage is limited to linear devices. To extend its usefulness to non-linear devices, some simplification techniques have been proposed [1, 24]. In these approaches, non-linear parameters are decomposed into a group of parameters, and each group is evaluated with less computational complexity. However, the test accuracy may suffer from this approximation.

In [12, 29, 74], the approach of alternate test has been proposed. Instead of using a typical sine wave, a specially crafted stimulus which is generated using AC, DC and transient signals is applied to DUTs and its response is characterized through *response feature extraction*. The extracted response features are fed to a mapping module which generates all the desired test specification values. The test input is optimized to excite potential failure sources in a device, and the feature extractor is selected so that the obtained features accurately represent the performance of the device with minimum impact on overall performance and hardware cost. The mapping module is designed to reconstruct the performance parameters from the obtained features. Due to absence of accurate models of complex analog circuits, the design of the mapping module relies on statistical approaches such as non-linear regression techniques. The difficulties with applying alternate test in complex analog

and RF circuits lies with the choice of models. For some linear circuits, the modeling may be straightforward (transfer function); however, in general, it is very difficult to develop accurate model which includes all the design parameters. In addition, a lack of reliable metric for the generated test input makes it difficult to measure device testability, and thus extensive simulation may be required.

In most of the aforementioned approaches, issues in testing of dynamic parameters such as gain, signal-to-noise ratio, and signal to total harmonic distortion are discussed. These parameters describe the effect of the signal channel on the quality of transmitted signal such as voice and modulated data [14]. In [22, 45, 56], testing methodologies of intrinsic parameters of data converters are studied. The intrinsic parameters depend on device implementation and its application. A common intrinsic parameter of data converters are integral nonlinearity (INL) and differential nonlinearity (DNL). INL and DNL values are often used to represent the static transfer characteristics of data converters. They are commonly referred to as static parameters. Generally, static parameter testing requires much larger samples and longer test time than dynamic parameter testing as it involves the measurement of every code transition. As the resolution of a device increases, the test time also increases. There has been research to find the correlation between the static parameters and dynamic parameters, and replace expensive static tests with dynamic tests [6, 10, 23]. However, the analysis is only limited to INL estimation, and thus DNL errors may not be detected. In [35, 56], a test approach for

precision ADCs using low-linearity ramp signals is discussed. The main goal of this approach is to relax the requirement on the source linearity for ADC test while maintaining high test accuracy. An imprecise continuous ramp signal and its shifted version are applied to ADCs under test and their correlation is used to estimate INL and DNL errors. This method requires an analog ramp generator and a stable voltage shifter. In [45], a linearity testing technique using an imperfect quantized ramp signal with finite resolution is proposed. The finite resolution is compensated by an interpolation technique. An interpolation technique is also used in [22, 73]. The accuracy of these techniques relies on the quality of the pre-assumed statistical distribution of noise.

ADCs and DACs are common modules in many mixed-signal SOCs, as they provide the interface between digital processing system and a real analog signal. The loopback test scheme is a common DFT approach for testing such mixed-signal SOCs [11, 63, 64, 69, 71, 79]. In a loopback test mode, a DUT is reconfigured in a mode that loops the output of the DACs back into the input of the ADCs. The DUT in a loopback mode is stimulated with digitized signals like digital circuit testing, and also the response is digitized samples. This approach provides efficient way to test analog systems with traditional digital methodologies. However, achieving high test coverage on a system in the loopback mode is a hard problem due to the fault masking problem. The fault masking problem results from the uncorrelated interaction between non-functionally related components in loopback mode. The combination of seriously degraded components in one of the functional paths and overqualified

components in another functional path, may result in misinterpretation of the loopback response. Therefore the loopback response does not directly represent the functional specifications of individual blocks or paths under test. The pass/fail decision based on the pure loopback test may lead to serious yield loss and low test accuracy since it is not made in the performance parameter domain where the specifications are clearly defined. At the same time, it may not be possible to perform the compensation tests for marginal DUTs [29] due to the difficulties of directly evaluating functional specifications. In addition, its utilization in diagnosis may be limited to locating an error to the loop rather than to a functional block.

Achieving high test coverage with loopback test scheme has been a major goal for years. One of earliest examples is a Hybrid Built-In Self Test (HBIST) technique [50]. Random sequences generated from Linear Feedback Shift Registers (LFSRs) are used for test inputs to a system in a loopback mode. The output response is compacted through similar LFSR-based signature analyzer. This method realizes a pure self-test using existing digital circuit. However, due to environmental noise and inherent circuit noise, reproducible signature cannot be obtained with this traditional digital-like signature analysis. More effective approach for signature analysis is found to be an accumulator [49, 62], which sums the magnitude of output response. In this approach, the signature is compared against a tolerable range of good signatures to account for acceptable changes in the output response due to noise. However, these approaches have certain limitations that the test result

cannot be readily interpreted into design specifications. Another example is Mixed Analog Digital BIST (MADBIST) [71]. The ADC is tested by on-chip pulse density modulator, and then the DAC is tested with the loopback configuration. Once the ADC and DAC are both verified, other analog circuitry is tested by placing it between the ADC and DAC. The limitation with this approach is design cost of an elaborated test input generator for the ADC, and the test time due to its partitioned test procedure. The dedicated test input generator has been removed in [79, 80]. Instead, the responses of internal nodes are observed in addition to primary outputs, and statistical equations which correlates the obtained signatures to the performance of individual ADCs and DACs are derived. The usefulness of this approach is, however, limited to certain types of mixed-signal circuits such as a Delta-Sigma converter.

Chapter 3

Specification-based BIST scheme using Time-Encoded Signature (TES) Generation

A traditional analog testing is widely based on sampling theorem (DSP-based test), where an output analog signal is reconstructed from the its amplitude samples taken uniformly at or above the Nyquist rate. DSP-based testing allows us to apply test inputs of many tones at the same time, and to separate the phase and gain of each tone from the output response. This separation provides us considerable advantages over non-DSP-based measurements. Firstly, many AC parametric tests can be performed in parallel with a single test application. Also, undesired signal components such as noise and harmonic components are readily identified [14]. This approach, however, is quite expensive in terms of hardware complexity [54]. The resolution and accuracy of quantizer are key factors in determining overall test accuracy, and in particular, in view of BIST, on-chip implementation of high precision quantizers is almost impractical to due the reliability issues as well as the design cost.

As an alternative representation for analog signals, time-encoding technique has been introduced [41, 77]. A time encoding is the time domain rep-

resentation of an analog signal as a sequence of strictly increasing times. The amplitude information is encoded into a time sequence, and its inverse process is performed in a digital domain. In this chapter, the efficient BIST implementation of time-encoding technique is explored. The Time-Encoded Signature (TES) is a compacted representation with much smaller parameters than a classical time-encoded sequence and a DSP-based sampled sequence. While a classical time encoding technique aims at perfect recovery of arbitrary analog signals, the TES is designed to contain the performance information of the output response of analog circuits to a known test input such as a step and sinusoid signal. The aliasing problem which may be caused by the severe compaction can be avoided by exploiting inherent statistical correlation between the process parameters and TES. The TES can be directly used for on-chip go/no-go decision by comparing the TES against its pre-defined tolerance limits. Furthermore, the Time-Encoded Signature Decoder(TESD) presented in this thesis decodes the obtained TES into performance parameters, thus allowing us to classify DUTs directly in the specification domain.

3.1 Test Stimulus Selection

As discussed earlier, the advantage of DSP-based testing is the ease of multi-tone testing and a significant test time reduction. However, the generation of a multi-tone test input may be difficult in a BIST environment. As an alternative, a step signal is often used as a test input for a Linear Time Invariant (LTI) analog circuits [8, 16, 66, 75]. As a step signal is composed of many

frequency components, LTI systems can be accurately characterized with its output response. Consider the transfer function of a second-order continuous time filter.

$$H(s) = \frac{K}{s^2 + (\omega_p/Q)s + \omega_p^2} \tag{3.1}$$

where Q, ω_p and K are the quality factor, the center frequency and the gain respectively. The time-domain output for an input step of a unity gain, $s(t)$ is

$$s(t) = K\left[1 - \frac{\omega_n}{\omega_d}e^{-\sigma t}sin(\omega_d t + \phi)\right]u(t) \tag{3.2}$$

where $\phi = arctan(\sqrt{4Q^2 - 1})$, $\omega_d = \omega_p\sqrt{1 - 1/4Q^2}$ and $\sigma = \omega_p/2Q$. It can be noted that the step response $s(t)$ is composed of Q, ω_p and K which are key parameters to determine the performance of analog circuits.

One of major difficulties in using the step response of analog circuits is long test time. The test time is determined by the settling time of the step response and it can be a few hundreds of milliseconds depending on the application. The measurement uncertainty may further increase the test time as the response need to be measured multiple times. In addition, the reconstruction of the transfer function from the step response requires a high precision quantizer which obviously adds substantial hardware cost.

The following sections will discuss how to reduce the test time by using a high-speed pulse and how to extract performance features based on the TES and TESD methodologies.

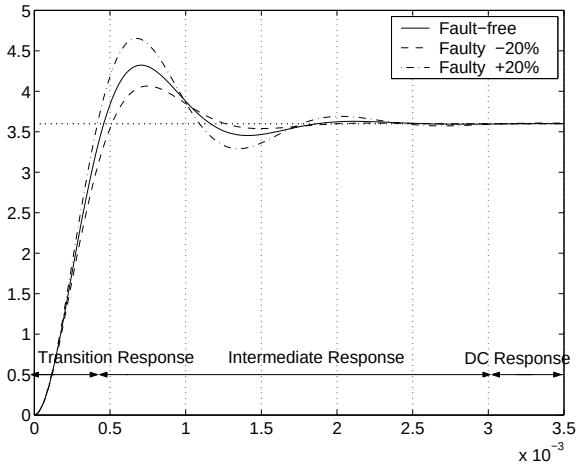
3.2 Accelerating Fault Detection by Speeding Up Periodic Pulses

As shown in Figure 3.1(a), the step response is composed of three parts. One is the transition response to a positive or negative step change which can be assumed to include many frequency components. The second is the intermediate response which is in a form of ringing and overshoot. The third is the DC response.

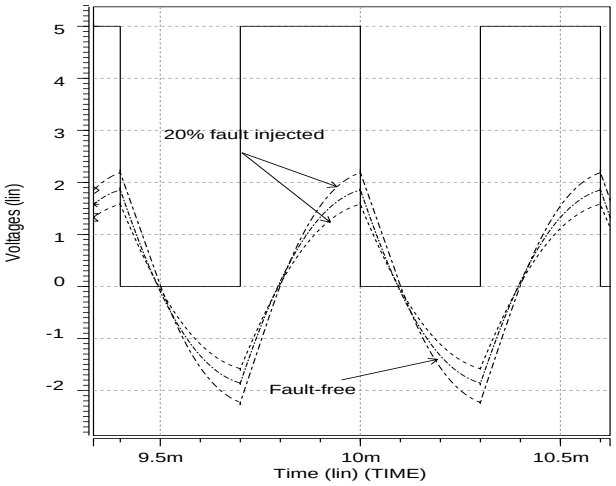
To reduce test time, the compressed step response to short pulses is measured. In other words, a part of the step response is observed and the rest of it is discarded by applying the pulse whose width is shorter than the DUT's settling time. Figure 3.1(b) shows the compressed response of the transfer function given in Equation 3.1, for a short pulse. Only the transition response and/or a part of the intermediate response are activated, and are periodically repeated. As the pulse width decreases, some faults may not be detected as some faults may not be fully responded for the short period. Thus, determining the proper pulse width is very crucial for high test coverage. The effects on the fault detection for various pulse widths are discussed in Section 3.5.

3.3 Time-Encoded Signature (TES)

The TES is composed of the rise time, peak time and slope of the compressed response. Simple comparators capture the compressed response and compare it with two reference voltages. For the resulting digital sequences $s_1(n)$ and $s_2(n)$, a bitwise difference is performed through a digital XOR gate,



(a) Normal Step Response



(b) Compressed Step Response

Figure 3.1: Normal and Compressed Step Response

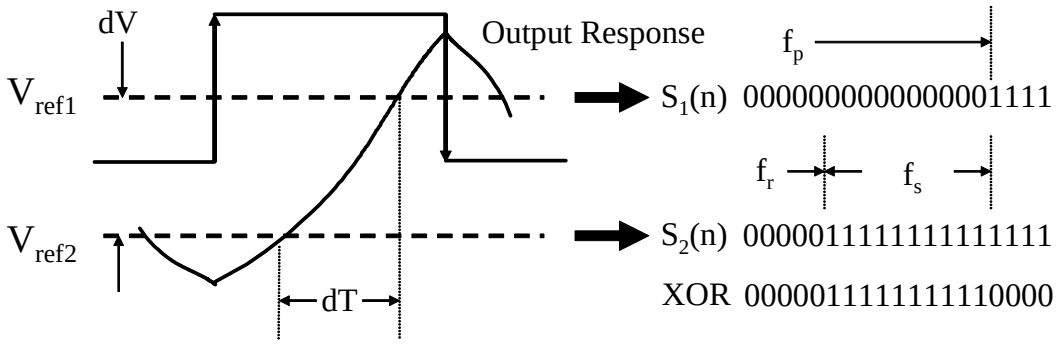


Figure 3.2: An Example for Slope Detection Technique

and its output sequence is collected in the digital counters along with the $s_1(n)$ and the $s_2(n)$. Let's consider an example shown in Figure 3.2. The number of zeros in the $s_1(n)$ represents the amount of time to reach V_{ref1}, and the first signature f_r is generated by counting the number of zeros in the $s_1(n)$, which corresponds to the rise time of the response. Similarly, the second signature f_p which represents the peak time of the response, can be calculated by counting the number of zeros in the $s_2(n)$. Finally, the third signature f_s which represents the slope of the response, can be determined by the bitwise difference between $s_1(n)$ and $s_2(n)$. The TES signature, f_r, f_p and f_s can be formulated as

$$\begin{aligned} f_r =& NS - \sum_{k=1}^{NS} s_1(k) \\ f_p =& NS - \sum_{k=1}^{NS} s_2(k) \\ f_s =& \frac{\Delta V}{\Delta T} = \frac{V_{ref2} - V_{ref1}}{\sum_{k=1}^{NS} s_1(k) XOR s_2(k)} \end{aligned} \tag{3.3}$$

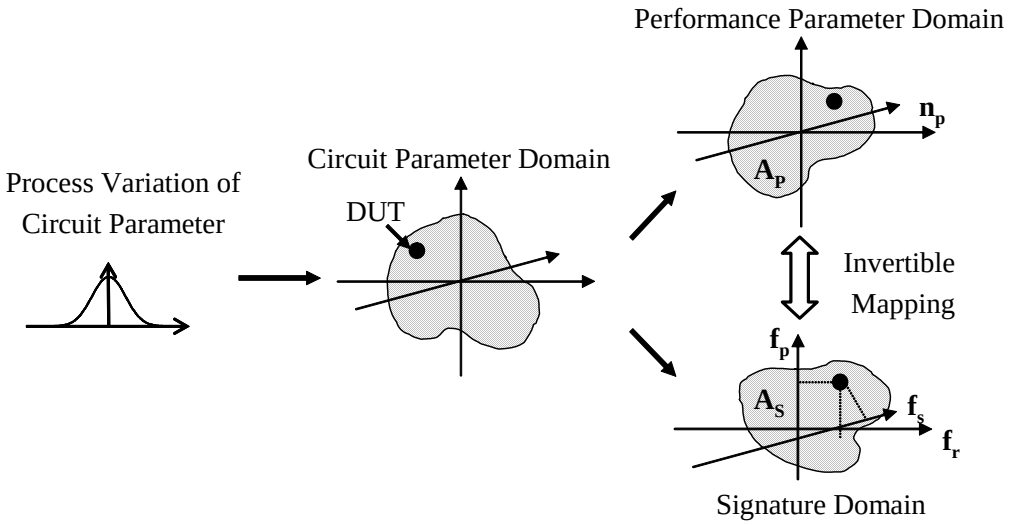


Figure 3.3: Acceptable Regions in Performance Parameter and Signature Domain

where NS is the total number of bits in the sequence.

3.3.1 Go/No-go Test based on TES and Tolerance Limit

This section describes how to apply the cost-effective TES to real manufacturing test and how the test cost can be reduced by removing expensive standard specification tests. As shown in Figure 3.3, a DUT ensemble is defined in the n_p dimensional performance parameter domain, P, by a set of n_p performance parameters such as DC gain, bandwidth and phase. An acceptable region, A_p, is defined by the specification limits of DUTs in the performance parameter space. Similarly, a DUT ensemble can be defined in the signature domain (TES domain). If a set of mapping functions given by Equation 3.4 exists and the functions are invertible, then the corresponding

acceptable region, A_s in the signature parameter space can also be defined.

$$f_{sp}^{i} : \mathbf{P} \rightarrow \mathbf{S}, \quad i = 1, \ldots, n_p \tag{3.4}$$

Therefore, if the signature values (f_r, f_p and f_s) of the DUT are within the acceptable region A_s, then the DUT is classified as a fault-free and vice versa. In this way, test can be performed simply by measuring the signature values rather than the complicated and expensive functional output. The A_s can be derived by Monte-Carlo simulation. Due to insufficient confidence of Monte-Carlo simulation and ill-conditioned mapping property of f_{sp}, it may be possible that fault-free DUTs are mapped into A_s and vice versa. It is called *fault aliasing* and it may lead to misclassification. Incorrect mappings of good devices cause yield loss and faulty devices cause test escape. The correlation factors are used to quantify the fault aliasing, and the results with the TES will be discussed in section 3.6.

3.4 Time-Encoded Signature Decoder (TESD) Design Using Statistical Regression Technique

Another way to evaluate the DUTs with the signature is to derive the mapping function f_{sp} rather than the A_s. This section discusses this alternative way to evaluate DUTs based on statistical regression technique.

3.4.1 Statistical Regression Technique

As discussed earlier, the signature-based test provides substantial advantages over a traditional analog test and DSP-based test. However, many

previous signature-based tests depend on defect-oriented pass/fail decision [49, 62]. In other words, the presence of a defect in the DUT results in the deviation of the signature values from their nominal values. This pure defect-oriented approach has certain limitations. Firstly, an extensive simulation is required to determine the acceptable region A_s, which is not usually required in a normal design phase. Secondly, the fault identification and location is another important goals of the test, however the signature cannot accomplish these purposes as the defect-oriented approach is intended to highlight the presence of a defect. In order to overcome these difficulties, a model or algorithm to translate the signature values into performance parameters is essentially required. However, nonlinear property of analog circuits and lack of a standard analysis tool of the compacted signature may complicate this problem.

A statistical non-linear regression model has been used to solve this problem [59, 74]. A model takes the form of an expansion in product of basis functions, where the number of basis functions as well as the parameters associated with each equation (product degree and knot locations) are determined by the data [25]. The data is composed of two classes. The first class is performance parameter values (response variables or dependent variables) that we ultimately want to know, and the second is the signature (predictor variables) which is independent variables for the regression model. Thus the regression technique allows us to obtain a optimal model for predicting the performance parameters, given the signature values. The non-linear regression allows us to model non-linear behavior of analog circuits.

3.4.2 Time-Encoded Signature Decoder (TESD)

The Time-Encoded Signature Decoder (TESD) is a statistical regression model whose predictor variables are the TES (f_p, f_s and f_r) and responses are the performance parameters. Instead of comparing the DUTs against the crafted acceptable region by simulation, the performance parameters predicted through the TESD is used. The advantage of the TESD is that the TES are now interpreted in the performance parameter space where the specification limits are clearly defined. This solves the problem of determining the acceptable region of the TES used for classification.

3.4.3 Implementation Flow

The major steps involved in the statistical regression model development and the practical implementation of the TES methodology, are depicted in Figure 3.4.

1. A set of DUT samples are obtained from Monte Carlo simulation or real dies manufactured from different lots and wafers. The use of samples from manufactured dies may improve the modeling accuracy by considering physical issues. The number of samples depend on the variation of circuit parameters.

2. For each sample, the response to the step input is captured and stored, and, at the same time, the specifications are measured using standard specification measurements.

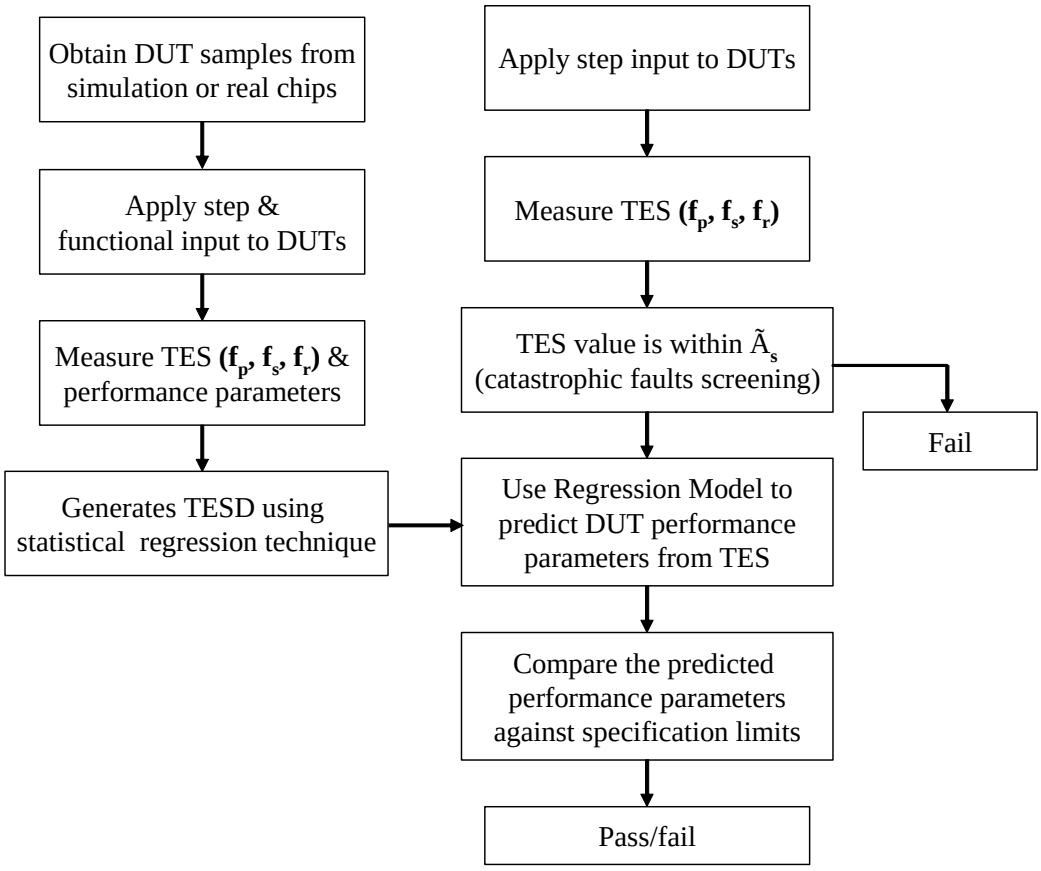


Figure 3.4: Implementation Flow of TES Methodology

3. Based on the collected data, the TESD is designed with a regression technique.

4. During production testing, only step input is applied, and the TES is measured.

5. Catastrophic faults can be detected by comparing the TES against the loose acceptable region $\tilde{A}_s$. This may be helpful for improving the accuracy of the TESD by reducing the predictor variable space.

6. The performance parameters of the DUT are predicted from TES, and pass/fail decision is made by comparing them against the specification limits.

3.5 Time-Encoded Signature BIST Implementation

This section discusses Time-Encoded Signature BIST scheme and implementation issues associated with trade-offs between the test accuracy and hardware cost.

3.5.1 Time-Encoded Signature BIST Scheme

Figure 3.5 shows a block diagram for the proposed Time-Encoded Signature BIST scheme. Linear Feedback Shift Register (LFSR) is exploited as a pulse generator, which is common in mixed-signal IC. A Time Division Multiplexing (TDM) [62] technique is also used to minimize the hardware overhead. As shown in Figure 3.6, the basic concept of the TDM comparator is to mul-

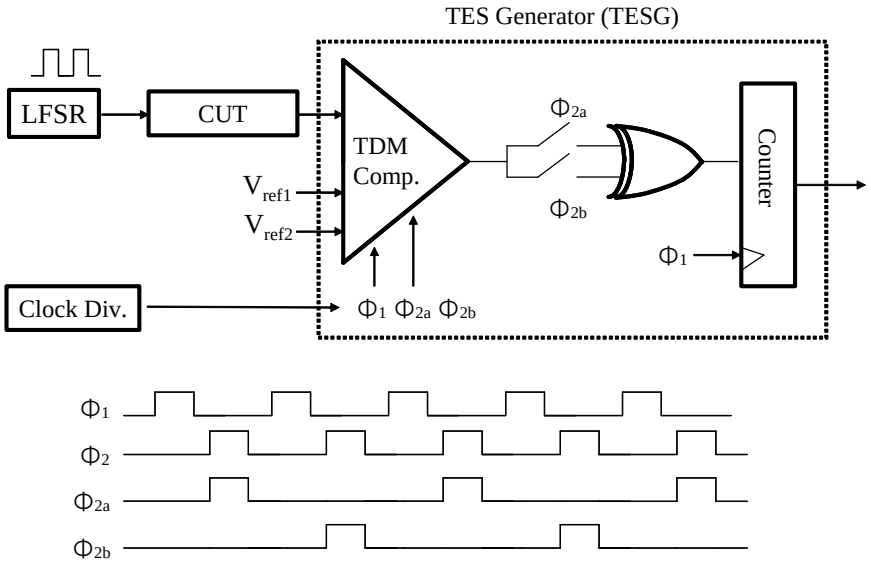


Figure 3.5: Time-Encoded Signature BIST Scheme

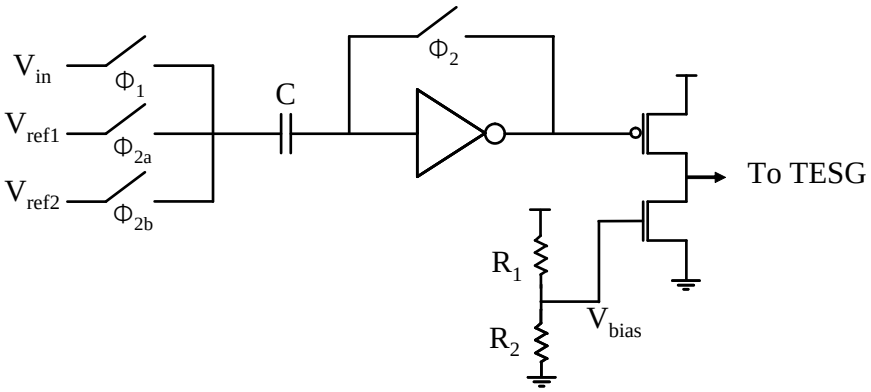


Figure 3.6: TDM Comparator

tiplex V_{ref1} and V_{ref2} as a reference voltage to the comparator. The input voltage V_{in} is captured on ϕ_1, and the comparator generates the comparison results according to the time slots ϕ_{2a} and ϕ_{2b}. Finally, the digital sequence $s_1(n)$ and $s_2(n)$ are generated from the comparator. The XOR gate performs a bitwise difference between the $s_1(n)$ and the $s_2(n)$, and its output sequence is collected in the digital counters along with the $s_1(n)$ and the $s_2(n)$. For Go/No-go test approach, digital comparators can be used to compare the signature values against the tolerance limits. For the TESD methodology, more computation hardware is required such as an adder and multiplier. If on-chip DSP or processor is available, it can be used for this computation. Otherwise, the signature values are transferred to outside PC or digital ATE. In either case, expensive mixed-signal testers are not required in this scheme.

3.5.2 Nonideal Effects in TESG

This section investigates implementation issues associated with the signature generation.

3.5.2.1 Effect of Resolution and Sampling Rate of Comparator

The basic idea of the TES methodology is the conversion of continuous analog signals into digital bit sequences which contain slope information. The key role of the comparators in the TES BIST scheme is to capture the rising time for the analog signal to reach a given threshold voltage. In this sense, the sampling rate of comparator (how often a signal is converted into a digital

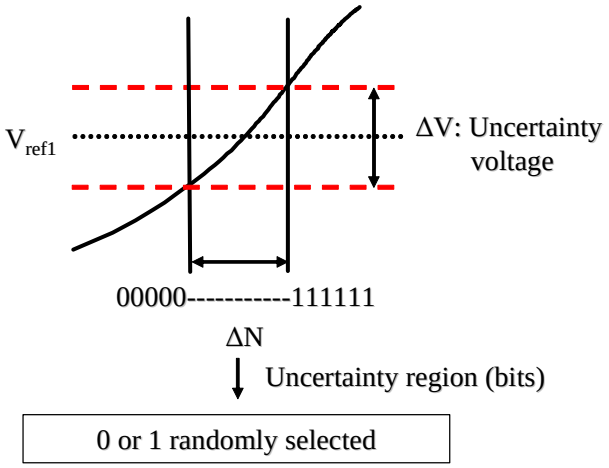


Figure 3.7: Effect of Resolution of Comparator

sequence) and the resolution may affect the precision of the signature which dominates overall test accuracy. Due to uncertainty in the amplitude of an analog signal and the sampling time of a comparator resulted from noise and jitter, the achievable resolution of the comparator is limited. Therefore, a time varying analog signal within certain ranges of the reference voltage, as shown in Figure 3.7, may not be converted correctly, resulting in uncertainty region (bits) ΔN in the signature values. ΔN can be formulated as follows.

$$\Delta N \propto \frac{\Delta V}{\text{slope}} \tag{3.5}$$

where ΔV is an uncertainty voltage. Equation 3.5 implies that ΔN is linearly proportional to ΔV.

Another factor which has a impact on the test accuracy is sampling rate. As more samples are obtained, effective number of bits which describe the analog signal behavior increases.

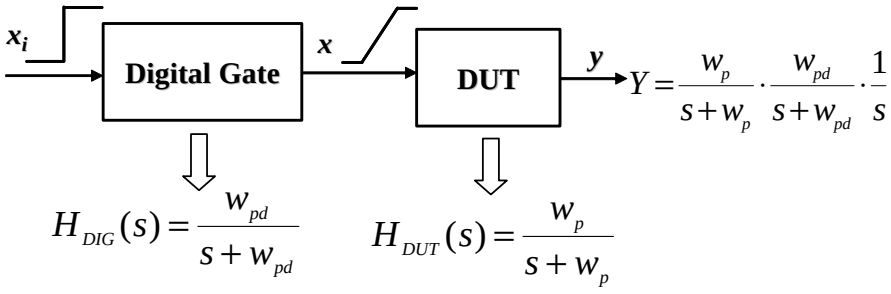


Figure 3.8: Nonideal Effect of Finite Rise Time of Step Input

3.5.2.2 Second-order Effect of High-speed Pulse

Several imperfections in a high-speed pulse input lead to inaccurate signature measurement. Due to the finite bandwidth of digital gates in LFSR, the high-speed pulse may have finite rise/fall time and ringing. Therefore, the output response to non-ideal step input can be re-written as follows [28].

$$Y(s) = \frac{K}{s^2 + (\omega_p/Q)s + \omega_p^2} \cdot \frac{V_{sat}}{s^2 + (\omega_{pd}/Q_d)s + \omega_{pd}^2} \cdot \frac{1}{s} \tag{3.6}$$

where ω_{pd} and Q_d are bandwidth and quality factor of the digital gate which drives the analog input respectively. V_{sat} is the final value of the step input. In order to see the nonideal effects of the finite rise or fall time of the step input, the digital gate is modeled as one-pole system as shown in Figure 3.8. Also, the transfer function of DUT is simplified into one-pole system since the digital gate of one real pole system has little impact on the ringing of the DUT. The step response of the system in Figure 3.8 can be represented as

$$Y(s) = \frac{\omega_p}{s + \omega_p} \cdot \frac{\omega_{dp}}{s + \omega_{dp}} \cdot \frac{1}{s} \tag{3.7}$$

and its time domain expression is

$$y(t) = 1 - \frac{\omega_{dp}}{\omega_{dp} - \omega_p} e^{-\omega_p t} + \frac{\omega_p}{\omega_{dp} - \omega_p} e^{-\omega_{pd} t} \tag{3.8}$$

As ω_{dp} goes to infinity, Equation 3.8 become ideal step response. Typically, ω_{dp} of digital gates, which is inverse of the transition time, is less than a few hundreds of pico-seconds, which correspond to tens of giga hertz. So it can be assumed that ω_{dp} is larger than ω_p. Based on this assumption, Equation 3.8 can be simplified as follows.

$$y(t) = 1 - e^{-\omega_p t} + \frac{\omega_p}{\omega_{dp}} e^{-\omega_{pd} t} \tag{3.9}$$

Therefore, the error due to the finite rise time of the step input is

$$Error(t) = \frac{\omega_p}{\omega_{dp}} e^{-\omega_{pd} t} \tag{3.10}$$

For example, the bandwidth of DUT is 1Mhz and the transition time of the step input is 100ps, then error is less than 100uV.

3.6 Simulation Results

The TES technique was applied to a continuous time state variable benchmark circuit [36] shown in Figure 3.9, whose quality factor and 3dB frequency are 1.11 and 765kHz and the settling time is 2.6ms. A set of DUT ensembles were generated by injecting the statistical variations in the value of the circuit parameters (passive components), and simulated using HSPICE. The frequency of clock $\phi 1$ and $\phi 2$ in Figure 3.5 was set to 1Mhz.

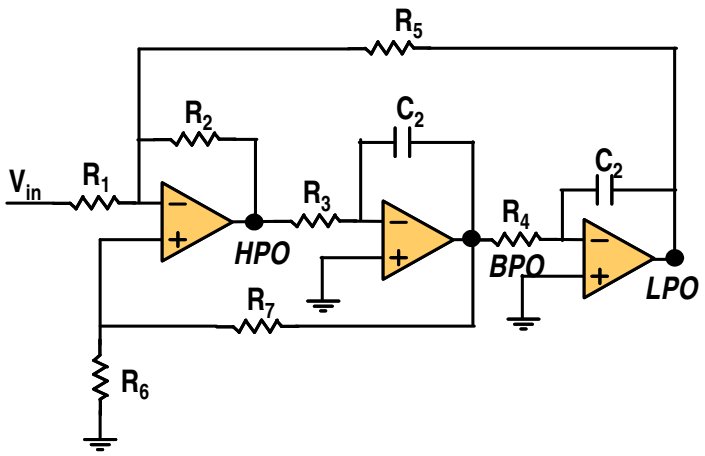


Figure 3.9: State-variable Active Filter

The following sections provide the simulation results for both Go/No-go test in which pass/fail decision was made based on the tolerance limits defined in the signature domain, and performance characterization using the TESD.

3.6.1 Go/No-go Test Results

A single-component fault and a ± 5% tolerance for all components was assumed, and a set of fault-free DUT ensembles were generated, and simulated in the TES BIST mode. The nominal values of the circuit parameters of the analog filter and their tolerance limits are shown in Table 3.1. The acceptable upper and lower bounds of the TES value were determined by the maximum and minimum value of the TES obtained from these fault-free DUTs. Table 3.2 summarizes the acceptable limits of the TES. A set of DUTs with ±20% parametric single fault was generated, and simulated with a test input of

Table 3.1: Nominal and Tolerance Limits of Circuit Parameters

	$R_1/R_2/R_3/R_4/R_5$	R_6	R_7	C_1/C_2
Nominal value	10k	3k	7k	20n
Tolerance Limits	8k-12k	2.4k-3.6k	5.6k-8.4k	16n-24n

Table 3.2: Acceptable Limits for TES Value (Pulse frequency was 1.7Khz)

	Acceptable limits
f_r	365-397
f_p	850-872
f_s	463-505

various pulse frequencies in the TES BIST mode. The obtained TES was compared against the tolerance limits defined above, and if the value was within the tolerance limits, then the DUT was classified as an undetected fault. Table 3.3 shows the list of undetected faults for various pulse frequencies. As pulse width increases, the number of undetected faults decreases, and finally at 1.25kHz, all faults were correctly detected. The simulation results were based on the observation of the bandpass output. However, this scheme can be applied to low-pass output or high-pass output. It may be interesting to note that we can observe a pattern in the undetected fault lists from 0.2msec to 0.4msec. A transition can be found at 0.5msec and once again, a pattern being different from the previous one can be observed from 0.6msec to 0.8msec. This is due to the fact that the sensitivity of faults is changed, as more intermediate response is added to the signature. Also, it can be seen that this method allows

Table 3.3: Undetected Faults (**UF**) for Various Pulse Frequency (R_1+ is +20% parametric fault, and R_1- is -20% parametric fault

Pulse freq.	Num. of UF	Undetected Fault List
5kHz	10	R_4+, R_4-, R_5+, R_5-, R_6+, R_6-, R_7+, R_7-, C_2+, C_2-
3.3kHz	8	R_4+, R_5+, R_5-, R_6+, R_6-, R_7+, R_7-, C_2+
2.5kHz	5	R_5+, R_5-, R_6+, R_6-, R_7+
2.0kHz	6	R_1-, R_4-, R_5-, R_6-, R_7+, C_2-
1.7kHz	3	R_2+, R_3+, C_1+
1.4kHz	1	R_2-
1.25kHz	0	
1.1kHz	0	
1.0kHz	0	

a trade-off between test time and high fault coverage.

3.6.2 Performance Characterization using TES

In this section, the simulation result for performance characterization using the TESD methodology is presented. The same second-order state variable benchmark circuit shown in Figure 3.9 was used. A set of 200 DUT ensembles was generated assuming 20% random deviations with normal distribution in the values of the circuit parameters. These DUTs were then simulated in the TES BIST mode and a standard specification test mode. The TESD was developed based on the performance parameters and TES obtained from 100 DUTs (Training sets), and for the remaining 100 DUTs the effectiveness of the TESD was validated by comparing the predicted performance parameters

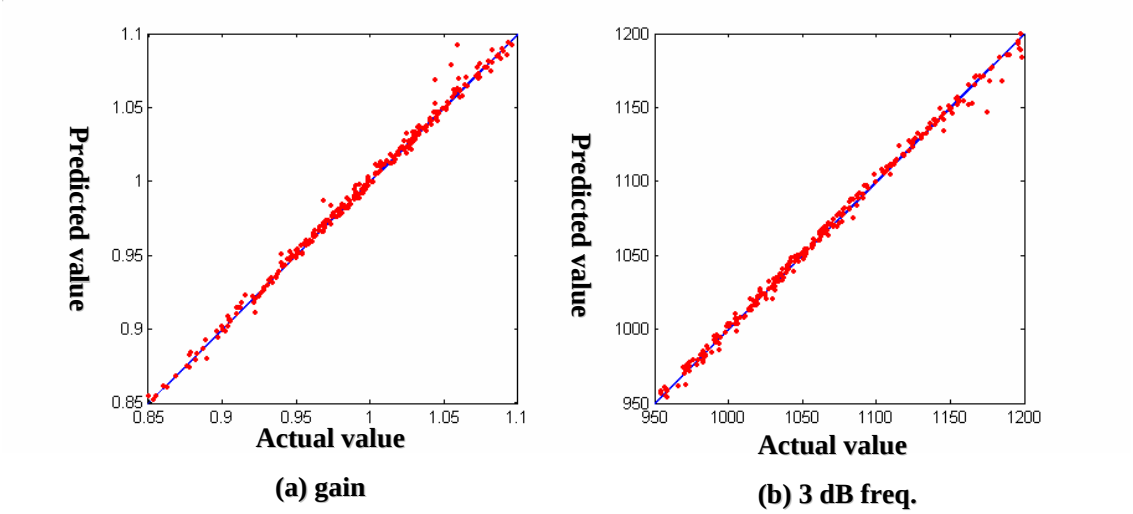


Figure 3.10: Comparison of Actual and Predicted values

against the actual values obtained from the standard specification tests. Figure 3.10 shows plots of the predicted versus the measured values of the gain and 3db frequency. Table 3.4 shows the correlation coefficients which represent the strength of the linear association between the predicted and actual performance parameters. The correlation coefficients were calculated based on the following equation.

$$r = \frac{\sum_1^{100}(x_i - \overline{x})(y_i - \overline{y})}{\sqrt{\sum_1^{100}(x_i - \overline{x})^2 \cdot \sum_1^{100}(y_i - \overline{y})^2}} \tag{3.11}$$

where x_i and y_i are the predicted and the actual performance parameters. This indicates that the predicted performance parameters have a high correlation with the actual value, and the TES methodology is relatively insensitive to fault aliasing.

Table 3.4: Correlation Coefficients

Performance Parameters	Correlation Coefficients
f_{3dB}	0.9977
Gain	0.9371

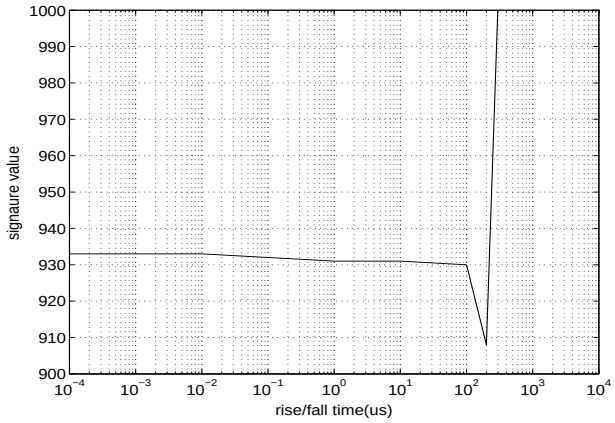


Figure 3.11: Variations of Signature for Finite Input Rise/Fall Times

3.6.3 Effects on Nonideal Test Input

As discussed earlier, a rectangular pulse generated from a LFSR has finite rise and fall times. The signature may be affected by these non-idealities. The DUTs were simulated with pulse input of various rise/fall time. In Figure 3.11, the variation of the signature values over a range of input rise times is plotted. From 100 psec to 100 nsec the deviation of signature was relatively small and at most 10us and over, the test failed. This result indicates a second-order effect caused by ringing can be avoided by applying a pulse of sufficiently slow slope.

Table 3.5: Comparison with Previous Work

	CSA [62]	POBT [59]	PQOBT [58]	TES
Test Input	Not required	Not required	Not required	Pulse
Hardware Overhead	2 comparators counter	Digitizer R + C	Digitizer R + C	2 comparators counter + XOR
Performance Prediction	No (but 100% fault coverage)	Yes	Yes	Yes (100% fault coverage
Prediction Correlation		94%		99.8%
Prediction Error			1.5%	0.3%
Test Time	2.2ms	2.2ms	>0.6ms	1.6ms

3.6.4 Comparison with Previous Work

Table 3.5 compares the TES methodology with previous BIST techniques. While the POBT and PQOBT are vectorless test techniques [58, 59], they require an expensive digitizer to sample the output response and additional hardware overhead associated with reconfiguring the DUT with passive components. The overhead of the output response measurement is significantly reduced in the case of the TES and CSA techniques [62]; however the CSA has the limitation that it only provides Pass/Fail decision based on tolerance band comparison, not the performance parameters in data sheet. In addition, the TES methodology provides much more accurate prediction than the POBT and PQOBT. While the prediction correlation of the POST and the prediction error of the PQOBT are 94% and 1.5% respectively, the TES provides 99.8% of the prediction correlation and 0.3% of the prediction error.

Also, the test time has been reduced compared to other techniques.

Chapter 4

Spectral Prediction for Specification-Based Loopback Test

In the previous chapter, a Built-in test technique for embedded analog blocks using existing on-chip digital circuits has been investigated. For a device which includes Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs), a different test strategy can be taken, in which the ADCs and DACs are used for test input generation and output acquisition. In this configuration, a DUT is reconfigured in a mode that loops the output of the DACs back into the input of the ADCs. This test strategy is called a loopback-based test [11, 63, 69, 71, 79]. The loopback-based test enables much more efficient testing using traditional digital methodologies, as it eliminates the need for any analog stimuli and measurements.

This method, however, suffers from fault masking caused by the uncorrelated interaction between non-functionally related components in loopback mode. The combination of seriously degraded components in one of the functional paths and overqualified components in another functional path, may result in misinterpretation of the loopback response. Therefore the loopback response does not directly represent the functional specifications of individual

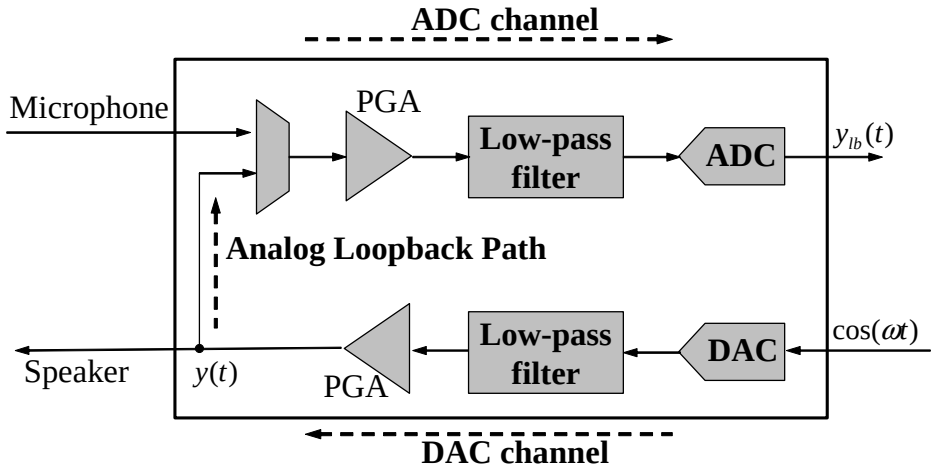


Figure 4.1: Conventional Analog Loopback Path of a Mixed-signal Circuit

blocks or paths under test. The pass/fail decision based on the pure loopback test may lead to serious yield loss and low test accuracy since it is not made in the performance parameter domain where the specifications are clearly defined. At the same time, it may not be possible to perform the compensation tests for marginal DUTs [29] due to the difficulties of directly evaluating functional specifications. In addition, its utilization in diagnosis may be limited to locating an error to the loop rather than to a functional block. Hence, the extraction of specifications of each functional path has become a crucial issue in loopback test. This chapter explores the loopback-based BIST scheme to overcome the fault masking problem.

4.1 Issues in Loopback Test

In order to better understand the fault masking issue in loopback tests, assume that a unit magnitude signal $\cos(\omega t)$ is applied to the non-linear DAC channel composed of the DAC, the lowpass filter and Programmable Gain Amplifier (PGA), as shown in Figure 4.1. We use t notation in digital domain for simplicity. Harmonic distortion considered is up to the third order. The output response $y(t)$ can be approximated by a Taylor expansion as follows [60].

$$y(t) = \alpha_1 \cos(\omega t) + \alpha_2 \cos^2(\omega t) + \alpha_3 \cos^3(\omega t) \tag{4.1}$$

where α_1, α_2 and α_3 are the first, second and third Taylor coefficients. Equation 4.1 can be expanded with harmonic coefficients as follows.

$$y(t) = (\alpha_1 + \frac{3\alpha_3}{4}) \cos(\omega t) + \frac{\alpha_2}{2} \cos(2\omega t) + \frac{\alpha_3}{4} \cos(3\omega t) \tag{4.2}$$

As shown in Figure 4.1, suppose this distorted and noisy analog signal $y(t)$ be loopbacked to the ADC channel, then the loopback response $y_{lb}(t)$ can be expressed as

$$\begin{aligned} y_{lb}(t) = (\beta_1\alpha_1) \cos(\omega t) + (\beta_1\alpha_2 + \beta_2\alpha_1^2) \cos^2(\omega t) \\ + (\beta_1\alpha_3 + 2\beta_2\alpha_1\alpha_2 + \beta_3\alpha_1^3) \cos^3(\omega t) \end{aligned} \tag{4.3}$$

where β_1, β_2 and β_3 are the first, second and third harmonic coefficients of the ADC channel respectively.

The common way to quantify the non-linearity of analog circuits is to identify the harmonic coefficients α_1, α_2, etc., or their sum [60]. However, it can be observed from Equation 4.3 that the characterization of harmonic

coefficients (or Taylor coefficients) of $y_{lb}(t)$ cannot provide the solution for α_i, unless the values of β_i are exactly identified.

In addition to the harmonic distortion, noise is a key parameter in mixed-signal circuits. Assume that $N_\alpha(f)$ is Power Spectral Density (PSD) of a pure noise input to the ADC channel, which is generated by the DAC channel, and $N_\beta(f)$ is the PSD of the ADC channel. Further assume that the noise of the DAC and the ADC channel are uncorrelated. The output referred noise of the loopback can be expressed as follows.

$$\overline{v_{lb}^2} = \int_0^\infty K N_\alpha(f) df + \int_0^\infty N_\beta(f) df \tag{4.4}$$

where K is the overall gain of the DAC and ADC channel. As can be seen from Equation 4.4, $\overline{v_{lb}^2}$ is the sum of noise of the ADC and the DAC channel, and any excessive value of noise in one channel can be masked by an overqualified performance of the other channel.

In summary, as the distortion and noise of two-cascaded sub-systems are additive, a standard DSP-based approach cannot provide the performance parameters of each signal channel.

4.1.1 Example of Issues

Consider a simple analog loopback configuration shown in Figure 4.1. A set of 2200 DUT ensembles was generated by introducing statistical variations into the noise and distortion that affect the SINAD of the ADC and the DAC channel, as well as the SINAD of the loopback response. The mean and

Table 4.1: DAC-ADC Specifications used for Classification

	Specification Limits		
	ADC	**DAC**	**Loopback Response**
SINAD	64dB	64dB	62.6dB

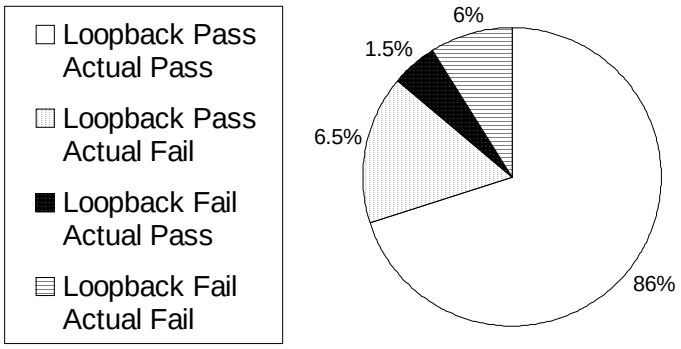


Figure 4.2: Test Escape and Yield Loss of Conventional Loopback Test

standard variation of the distribution of the obtained SINAD were approximately 66dB and 1.3dB respectively. In order to determine test limits of the loopback response, a set of 200 DUT ensembles was simulated in both loopback and normal mode, and the SINAD of individual ADC and DAC, and loopback response were measured. The only specification parameter considered for the classification was SINAD. The lower SINAD limit of the loopback response is determined by the minimum loopback SINAD of DUTs, which passes both the ADC and the DAC test. The upper limit is derived in a similar way. Table 4.1 summarizes the specification limits for the ADC, the DAC and the loopback response. The specification limit of the loopback response shown in Table 4.1 was compared against the measured SINAD of the remaining 2000 DUT

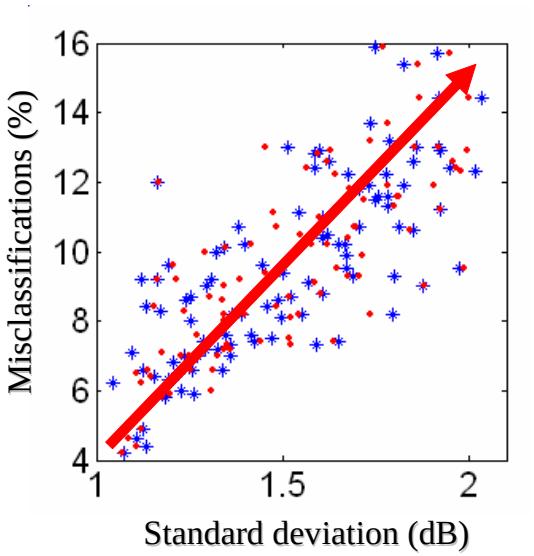


Figure 4.3: Misclassification versus Variation of SINAD

ensembles. Figure 4.2 shows the ratio of the misclassification for the conventional loopback test. 6.5% of DUTs which passed the loopback test turned out to be faulty in either the ADC or the DAC. This is due to the fault masking, which may cause a significant reduction in test quality. In addition, 1.5% of DUTs which passed the individual tests failed the loopback test. In fact, the misclassification ratio strongly depends on the variation of performance parameters of DUTs. The misclassification ratio with respect to variation of SINAD value of DUTs is plotted in Figure 4.3. It can be seen that wider variation of performance of DUTs results in more serious misclassification.

This result demonstrates that the loopback test alone cannot provide thorough production test and diagnosis. Therefore, the extraction of the char-

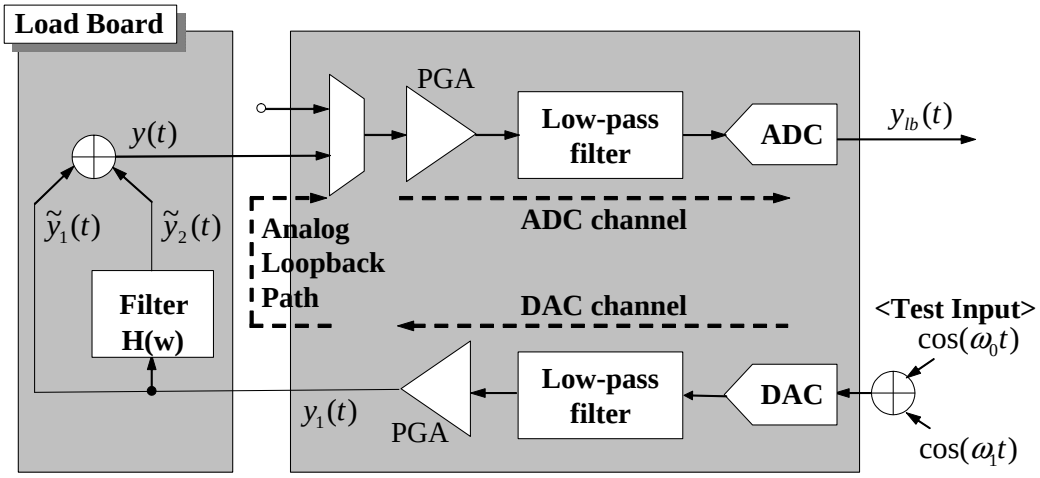


Figure 4.4: Proposed Loopback Test Scheme

acteristics of individual channels from the loopback response is required to improve the test quality.

4.2 Improved Loopback-based BIST for Dynamic Performance Characterization

The previous section discussed issues related to the fault masking problem found in the loopback test, and the difficulties in extracting the performance parameters of each signal path from the loopback response. In the following sections, the improved loopback-based BIST using a two-tone test input and an analog filter, which enables the accurate characterization of dynamic performance parameters of individual channels, is discussed.

4.2.1 Improved Loopback-based BIST Scheme

Figure 4.4 shows the proposed loopback architecture. The loopback path is connected externally to the die through a simple low-order filter and an analog adder on the Device Interface Board (DIB) [61]. In the proposed BIST scheme, a critical BIST block which requires high accuracy is located on the DIB, thereby high flexibility in the calibration process of the BIST block can be achieved and the characteristics of the accurately calibrated analog filter can be confidently used.

4.2.2 Harmonic Distortion Parameter Extraction

A digital bit sequence of two-tone cosine wave of frequency ω_0 and ω_1, is used as a test input and applied to the DAC in Figure 4.4 using either an on-chip DSP or an external digital ATE. The response of the Taylor series to a two-tone signal can be determined by expanding trigonometric identities. That is,

$$\begin{aligned} y_1(t) = &\sum_k \alpha_k \cos(k\omega_0 t) + \sum_l \alpha_l^{'} \cos(l\omega_1 t) \\ &+ \sum_{m,n} \eta_{m,n} \cos((m\omega_0 \pm n\omega_1)t) + \alpha_0 \end{aligned} \tag{4.5}$$

where α_k and $\alpha_l^{'}$ are harmonic coefficients of the DAC channel for frequency ω_0 and ω_1, and α_0 is DC value. $\eta_{m,n}$ are Intermodulation Distortion (IMD) coefficients. IMD is often generated when two or more tones are applied to non-linear devices simultaneously. ω_0 and ω_1 are assumed to be as close as possible to each other, such that the harmonic coefficients of $cos(k\omega_0 t)$ and

$cos(l\omega_1 t)$ are identical, i.e., $\alpha_k = \alpha_l^{'}$. In addition to the fundamental and harmonic components, the interaction of ω_0 and ω_1 produces IMD. ω_0 and ω_1 are chosen to be mutually prime, thus the IMD components do not overlap with the fundamental and harmonic components, i.e., $m\omega_0 \pm n\omega_1 \neq k\omega_0$ and $m\omega_0 \pm n\omega_1 \neq l\omega_1$ for any integer k, l, m and n [14]. Since the fundamental and distortion components are only of interest (as characteristic parameters), the IMD components will be ignored in deriving following equations. In addition, α_0 will be neglected, since the filter or PGA in the ADC channel will cancel the DC terms. Therefore, Equation 4.5 can be simplified as follows.

$$\tilde{y}_1(t) = \sum_k \alpha_k(\cos(k\omega_0 t) + \cos(k\omega_1 t)) \tag{4.6}$$

The filter in Figure 4.4 produces the secondary loopback input $\tilde{y}_2$ from $\tilde{y}_1$, which can be expressed as

$$\begin{aligned} \tilde{y}_2(t) = &\sum_k |H(k\omega_0)|\, \alpha_k \cos(k\omega_0 t + \theta_k) \\ &+ \sum_l |H(l\omega_1)|\, \alpha_l \cos(l\omega_1 t + \phi_l) \end{aligned} \tag{4.7}$$

where $H(\omega)$ is the transfer function of the filter which is

$$\begin{aligned} H(\omega)|_{w=k\omega_0} &= \gamma_k e^{j\theta_k} \\ H(\omega)|_{w=k\omega_1} &= \zeta_k e^{j\phi_k} \end{aligned} \tag{4.8}$$

Since in general the roll-off slope of the filter in the frequency domain is much sharper than the variation of distortion coefficients of the ADC and DAC, we assume that the values of γ_k and ζ_k are different even when ω_0 and ω_1

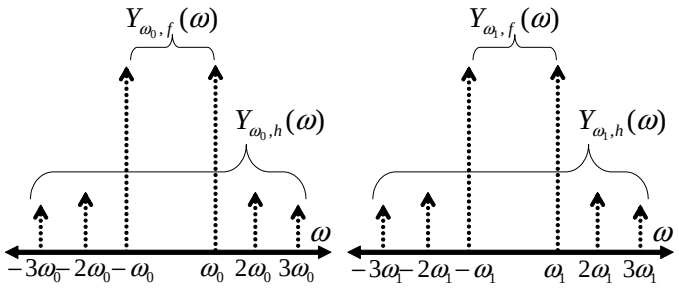


Figure 4.5: Fundamental and Harmonic components of $Y(\omega)$

are close to each other. We further assume that the specifications of the filter are characterized prior to the test, and γ_k, ζ_k, θ_k and ϕ_k are known values.

As shown in Figure 4.4, $\tilde{y}_2$ is added to $\tilde{y}_1$, and consequently we obtain the final input to the ADC channel $y(t)$. That is,

$$\begin{aligned} y(t) &= \tilde{y}_1(t) + \tilde{y}_2(t) \\ &= \sum_k (\alpha_k \cos(k\omega_0 t) + \gamma_k \alpha_k \cos(k\omega_0 t + \theta_k)) \\ &\quad + \sum_l (\alpha_l \cos(l\omega_1 t) + \zeta_l \alpha_l \cos(l\omega_1 t + \phi_l)) \end{aligned} \tag{4.9}$$

As shown in Figure 4.5, the frequency domain representation of $y(t)$, $Y(\omega)$ can be divided into four parts, fundamental and harmonic components of ω_0 and ω_1 as follows.

$$Y(\omega) = Y_{\omega_0,f}(\omega) + Y_{\omega_0,h}(\omega) + Y_{\omega_1,f}(\omega) + Y_{\omega_1,h}(\omega) \tag{4.10}$$

We use the Equation 4.1 to model the ADC channel with Taylor coefficients β_k, and the loopback response y_{lb} can be expressed as

$$y_{lb}(t) = \beta_1 y(t) + \beta_2 y^2(t) + \beta_3 y^3(t) \tag{4.11}$$

$y^2(t)$ in Equation 4.11 can be expressed as a convolution of $Y(\omega)$ in the frequency domain, which is

$$\mathcal{F}(y^2(t)) = Y^{'}(\omega) = Y(\omega) \otimes Y(\omega) \tag{4.12}$$

Since the convolution of ω_0 and ω_1 produces IMD in which we are not interested, these terms are ignored. Then Equation 4.12 becomes

$$\begin{aligned} Y^{'}(\omega) = &(Y_{\omega_0,f}(\omega) + Y_{\omega_0,h}(\omega)) \otimes (Y_{\omega_0,f}(\omega) + Y_{\omega_0,h}(\omega)) \\ &+ (Y_{\omega_1,f}(\omega) + Y_{\omega_1,h}(\omega)) \otimes (Y_{\omega_1,f}(\omega) + Y_{\omega_1,h}(\omega)) \end{aligned} \tag{4.13}$$

and can be expanded to

$$\begin{aligned} Y^{'}(\omega) = &\{Y_{\omega_0,f}(\omega) \otimes Y_{\omega_0,f}(\omega) + 2Y_{\omega_0,f}(\omega) \otimes Y_{\omega_0,h}(\omega) + Y_{\omega_0,h}(\omega) \otimes Y_{\omega_0,h}(\omega)\} \\ &+ \{Y_{\omega_1,f}(\omega) \otimes Y_{\omega_1,f}(\omega) + 2Y_{\omega_1,f}(\omega) \otimes Y_{\omega_1,h}(\omega) + Y_{\omega_1,h}(\omega) \otimes Y_{\omega_1,h}(\omega)\} \end{aligned} \tag{4.14}$$

The convolution of harmonic components $Y_h(\omega) \otimes Y_h(\omega)$ may be negligible. For example, the multiplication of the second and third harmonics will produce trivial magnitudes. While it can be included for better accuracy, it will be ignored for computational simplicity.

Then, Equation 4.14 becomes

$$\begin{aligned} Y^{'}(\omega) = &Y_{\omega_0,f}(\omega) \otimes Y_{\omega_0,f}(\omega) + 2Y_{\omega_0,f}(\omega) \otimes Y_{\omega_0,h}(\omega) \\ &+ Y_{\omega_1,f}(\omega) \otimes Y_{\omega_1,f}(\omega) + 2Y_{\omega_1,f}(\omega) \otimes Y_{\omega_1,h}(\omega) \end{aligned} \tag{4.15}$$

Similarly, the frequency response $Y^{''}(\omega)$ of $y^3(t)$ can be obtained, and the frequency response $Y_{lb}(\omega)$ of $y_{lb}(t)$ is

$$Y_{lb}(\omega) = \beta_1 Y(\omega) + \beta_2 Y^{'}(\omega) + \beta_3 Y^{''}(\omega) \tag{4.16}$$

Consequently, the frequency response of the fundamental and harmonic components of $y_{lb}(t)$ can be expressed as

$$\begin{aligned}
Y_{lb}(\omega_0) &= \beta_1\hat{\alpha_1} + \beta_2/2(\hat{\alpha_1}\hat{\alpha_2}) \\
&\quad + \beta_3/8(3\hat{\alpha_1}^3 + 2\hat{\alpha_1}^2\hat{\alpha_3} + 2\hat{\alpha_1}^2\hat{\alpha_2}) \\
Y_{lb}(2\omega_0) &= \beta_1\hat{\alpha_2} + \beta_2/4(\hat{\alpha_1}^2 + 2\hat{\alpha_1}\hat{\alpha_3}) \\
&\quad + \beta_3/4(3\hat{\alpha_1}^2\hat{\alpha_2} + \hat{\alpha_1}\hat{\alpha_2}\hat{\alpha_3}) \\
Y_{lb}(3\omega_0) &= \beta_1\hat{\alpha_3} + \beta_2/2(\hat{\alpha_1}\hat{\alpha_2}) \\
&\quad + \beta_3/8(\hat{\alpha_1}^3 + 4\hat{\alpha_1}^2\hat{\alpha_3} + 2\hat{\alpha_1}\hat{\alpha_2}^2) \\
Y_{lb}(\omega_1) &= \beta_1\check{\alpha_1} + \beta_2/2(\check{\alpha_1}\check{\alpha_2}) \\
&\quad + \beta_3/8(3\check{\alpha_1}^3 + 2\check{\alpha_1}^2\check{\alpha_3} + 2\check{\alpha_1}^2\check{\alpha_2}) \\
Y_{lb}(2\omega_1) &= \beta_1\check{\alpha_2} + \beta_2/4(\check{\alpha_1}^2 + 2\check{\alpha_1}\check{\alpha_3}) \\
&\quad + \beta_3/4(3\check{\alpha_1}^2\check{\alpha_2} + \check{\alpha_1}\check{\alpha_2}\check{\alpha_3}) \\
Y_{lb}(3\omega_1) &= \beta_1\check{\alpha_3} + \beta_2/2(\check{\alpha_1}\check{\alpha_2}) \\
&\quad + \beta_3/8(\check{\alpha_1}^3 + 4\check{\alpha_1}^2\check{\alpha_3} + 2\check{\alpha_1}\check{\alpha_2}^2)
\end{aligned} \tag{4.17}$$

where

$$\begin{aligned}
\hat{\alpha_k} &= \alpha_k + \gamma_k\alpha_k e^{j\theta_k} \\
\check{\alpha_k} &= \alpha_k + \zeta_k\alpha_k e^{j\phi_k}
\end{aligned} \tag{4.18}$$

In summary, $Y_{lb}(k\omega_0)$ and $Y_{lb}(k\omega_1)$ (characteristic parameters) can be calculated by performing Fast Fourier Transform (FFT) on the measured loop-back response. Therefore, given γ_k, ζ_k, θ_k and ϕ_k, we can estimate α_k and β_k from Equation 4.17 and the harmonic distortion of the ADC and DAC channel can be quantified separately.

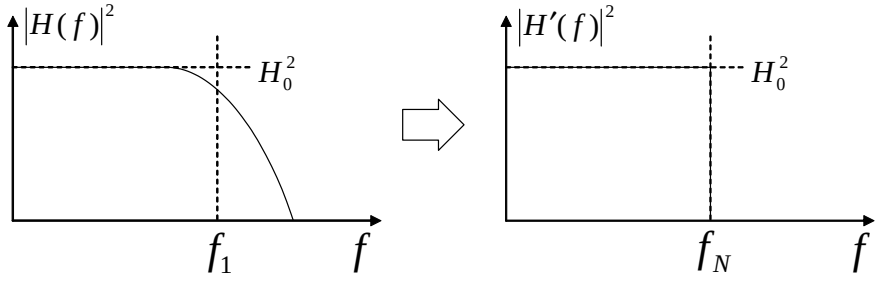


Figure 4.6: Equivalent Noise Bandwidth (f_1 is 3dB cutoff frequency)

4.2.3 Noise Parameter Extraction

In the proposed scheme shown in Figure 4.4, the output referred noise of y_{lb} in Equation 4.4 can be re-written as follows.

$$\begin{aligned}\overline{v_{lb}^2} = &\int_0^\infty KN_\alpha(f)df + \int_0^\infty N_\beta(f)df \\ &+ \int_0^\infty KN_\alpha(f)\left|H(f)\right|^2 df + \int_0^\infty KN_H(f)df\end{aligned} \tag{4.19}$$

where $N_H(f)$ is the PSD of the filter, and we use the f notation rather than ω for simplicity. As in Equation 4.4, the output referred noise $\overline{v_{lb}^2}$ in Equation 4.19 contains the noise generated from the ADC channel and the DAC channel. Also, it includes the noise generated from the filter and the scaled noise of the DAC by the transfer function of the filter. In order to decompose Equation 4.19 with respect to frequency bands, we use the *equivalent noise bandwidth* [28]. The equivalent noise bandwidth f_N is chosen to give the same total output noise voltage as the original block when the same input noise voltage is applied. As shown in Figure 4.6, the frequency response of the filter $|H(f)|^2$ can be approximated as a simple gain-frequency characteristics with

abrupt band edges, $|H^{'}(f)|^2$, where the magnitude is the same as the low frequency gain of $|H(f)|^2$. Thus, we can approximate the complicated integral with $|H(f)|^2$ in Equation 4.19 into

$$\int_0^\infty N_\alpha(f) \left|H^{'}(f)\right|^2 df \approx H_0^2 \int_0^{f_N} N_\alpha(f) df \tag{4.20}$$

Accordingly, Equation 4.19 can be simplified into

$$\begin{aligned} \overline{v_{lb}^2} \approx & \int_0^{f_N} K N_\alpha(f) \left|H^{'}(f)\right|^2 df \\ & + \int_0^\infty (K N_\alpha(f) + N_\beta(f) + K N_H(f)) df \end{aligned} \tag{4.21}$$

$\overline{v_{lb}^2}$ in Equation 4.21 can be divided into two components with respect to the frequency ranges. $\overline{v_a^2}$ is total noise of y_{lb} in the frequency range $[0\ f_N]$ and $\overline{v_b^2}$ is the total noise in the frequency range $[f_N\ \infty]$.

$$\begin{aligned} \overline{v_a^2} &= K(1+H_0^2) \int_0^{f_N} N_\alpha(f) df + \int_0^{f_N} (N_\beta(f) + K N_H(f)) df \\ \overline{v_b^2} &= K \int_{f_N}^\infty N_\alpha(f) df + \int_{f_N}^\infty (N_\beta(f) + K N_H(f)) df \end{aligned} \tag{4.22}$$

$\overline{v_a^2}$ and $\overline{v_b^2}$ are readily computed from the measured loopback response. If we assume that the spectral content of the noise is white, then the ratio of $\int_0^{f_N} N_\alpha(f) df$ and $\int_{f_N^\infty} N_\alpha(f) df$ is constant. Also, it can be similarly applied to the integral of the ADC noise. Therefore, Equation 4.22 becomes

$$\begin{aligned} \overline{v_a^2} &= K(1+H_0^2) \int_0^{f_N} N_\alpha(f) df + \int_0^{f_N} (N_\beta(f) + K N_H(f)) df \\ \overline{v_b^2} &= Kc \int_0^{f_N} N_\alpha(f) df + c \int_0^{f_N} N_\beta(f) + \int_{f_N}^\infty K N_H(f) df \end{aligned} \tag{4.23}$$

where

$$c = \frac{\frac{f_s}{2} - f_N}{f_N} \tag{4.24}$$

where f_s is the sampling frequency of the ADC. Therefore, if K, $H(f)$, and $N_H(f)$ are given, $\int_0^{f_N} N_\alpha(f)df$, $\int_0^{f_N} N_\beta(f)df$, $\int_{f_N}^{\infty} N_\alpha(f)df$ and $\int_{f_N}^{\infty} N_\beta(f)df$ can be calculated. Consequently, the noise parameters of the ADC and DAC channel can determined.

4.2.4 Non-linear Regression using a Spectral Predictor

The target equations to extract harmonic distortion and noise parameters are highly nonlinear. In fact, it may be more difficult if higher order harmonic distortion is considered such as $Y_h(\omega) \otimes Y_h(\omega)$, 4th harmonic, 5th harmonic, etc. In addition, uncertainty of analog signals may cause an error in measurement, and the error can be propagated into the evaluation of the equations. In order to solve this type of nonlinear equations, a non-linear regression technique based on spectral predictors is used. Spectral powers at frequency bins which are used in Equation 4.23 and 4.17, are used as predictor variables. The response variables are the performance parameters such as THD, SNR and SINAD.

4.3 Alternate Test Scheme

In addition to the two-tone test scheme described thus far, it is also possible to apply two separate single tone signals. Two responses with the different weights, $Y_{\omega_0}(\omega)$ and $Y_{\omega_1}(\omega)$ are generated separately. The two loopback

responses are analyzed in a similar way, and the characteristic parameters can be derived. This test scheme may be more effective than the two-tone scheme when the harmonics are relatively small compared to noise, therefore their identification is difficult. This may occur in the two-tone test scheme since the power of harmonics tends to spread out to IMD bins, which we ignored for analysis. Also, a multi-tone signal more than two-tone can be used. The response of the multi-tone signal gives us more predictor variables, so that the accuracy in solving the nonlinear equations can be improved. However, when the multi-tone input is applied at the same time, the magnitude of frequency component will be lessened due to the limitations of the allowable input scales. This may cause an adverse effect on the signal integrity.

4.4 Experimental Results

This section presents both simulation and hardware measurements to validate the proposed technique. A MATLAB simulation using a two-tone input will be first presented, and hardware measurements using two single tone inputs performed on a commercial broadband modem (AD9865) will be followed.

4.4.1 Simulation Results

The spectral prediction technique presented in this chapter was applied to the mixed-signal system shown in Figure 4.4, which is composed of typical baseband transmit and receive sub-systems. In test mode, the DAC channel

Table 4.2: Mean and Standard Deviation of Prediction Errors of Simulations

Parameter	**DAC channel**		**ADC channel**	
	Mean	**STD.**	**Mean**	**STD.**
SNR (dB)	0.85dB	0.71dB	0.26dB	0.23dB
THD (dB)	0.07dB	0.07dB	0.29dB	0.31dB
SINAD (dB)	0.07dB	0.08dB	0.38dB	0.66dB

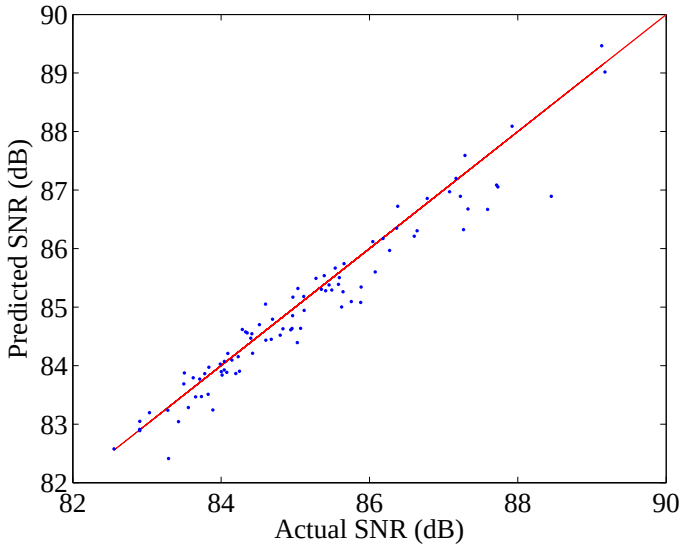
output was looped back to the ADC channel through the analog filter which was modeled as a first-order RC filter. A two-tone sine-wave whose harmonics and intermodulation harmonics do not overlap with each other was applied to the DUT. The frequencies were 97kHz and 83Khz. The number of sampling points was 2024. A set of 200 DUT ensembles was generated by introducing statistical variations with normal distribution in values of gain, random noise and harmonic distortion. Combinations of these values were also generated randomly. Among them, 100 ensembles (training sets) were simulated in normal and test mode, and the performance parameters of the DAC and ADC channel, and spectral predictors which were used to solve the nonlinear equations (mapping functions) were then obtained. The mapping functions were used to predict the performance parameters of the remaining DUT ensembles (validation sets). The performance parameters considered in this paper were the gain, Signal-to-Noise Ratio (SNR), Total Harmonic Distortion (THD) and Signal-to-Noise and Distortion Ratio (SINAD).

Table 4.2 provides the mean and standard deviation of prediction errors for the ADC and DAC channel performance. For SNR estimation of the ADC

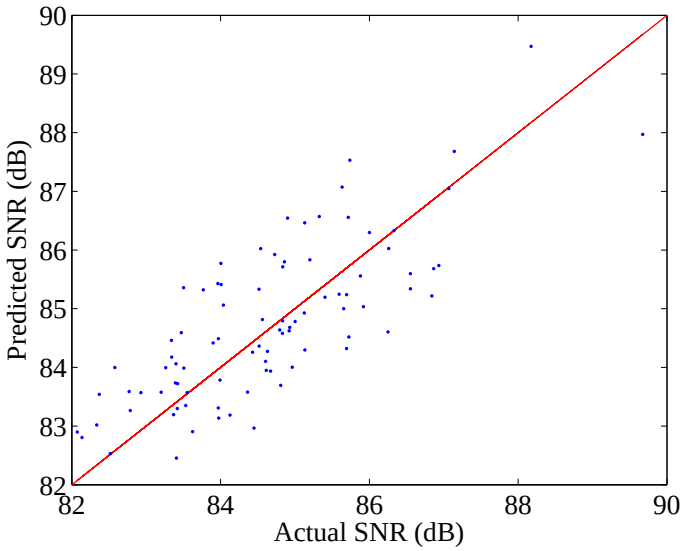
channel, the average of the differences between the actual SNR and the predicted SNR was 0.26dB, and for the DAC channel, it was 0.85dB. The reason for this gap in the prediction accuracy is that the amplitude response of $H(f)$ in Equation 4.20 is not, in fact, constant, and therefore its approximation to a constant value introduced errors in the estimation. On the other hand, as can be seen in Equation 4.23, N_α which determines the ADC channel noise is not multiplied by the transfer function of the filter. For THD estimation, the prediction errors of the ADC and DAC channel were 0.29dB and 0.07dB respectively. Unlike the case of SNR, the prediction errors of the DAC channel is less than the ADC channel. This is primarily due to the fact that the Taylor coefficients in Equation 4.17 needs extra process that convert them to harmonic coefficients so as to quantify harmonic distortion. It can be noted that we can derive harmonic coefficients of the ADC channel directly from Equation 4.17. The plot of the predicted versus the actual values of the DUT performance parameters are shown in Figure 4.7, Figure 4.8 and Figure 4.9.

4.4.1.1 Design Considerations of the Filter Circuit

Two design parameters of the filter, cutoff frequency (f_N) and filter orders, are investigated in this section. The cutoff frequency is an important parameter which may determine the test accuracy in this approach. If the cutoff frequency is too close to DC, the fundamental and harmonic components of the loopback response may be located in a deep transition band or stopband, so that they may be varied under the noise. In contrast, if it is too close to

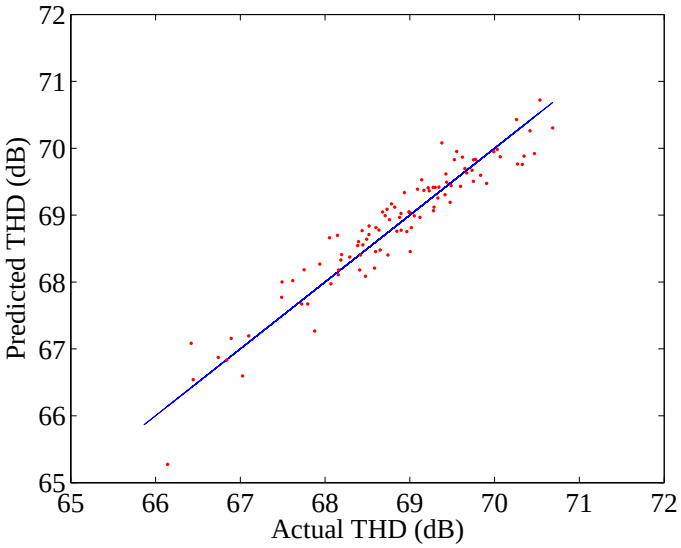


(a) Actual and Predicted ADC SNR

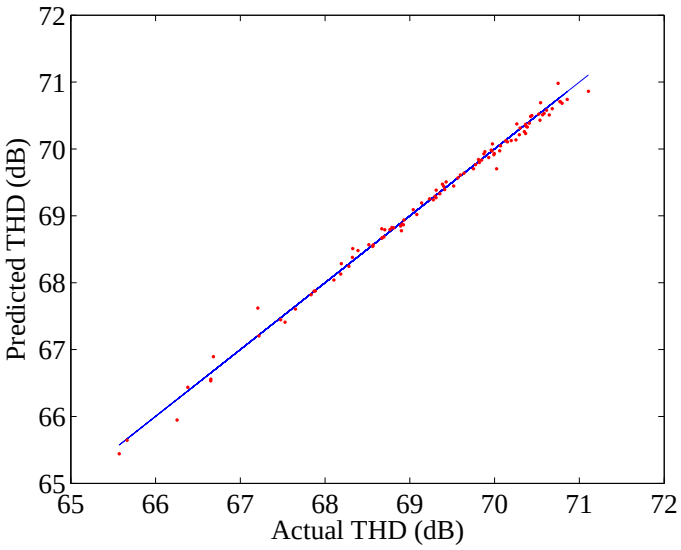


(b) Actual and Predicted DAC SNR

Figure 4.7: Comparison of Actual and Predicted SNR (Simulation Data)

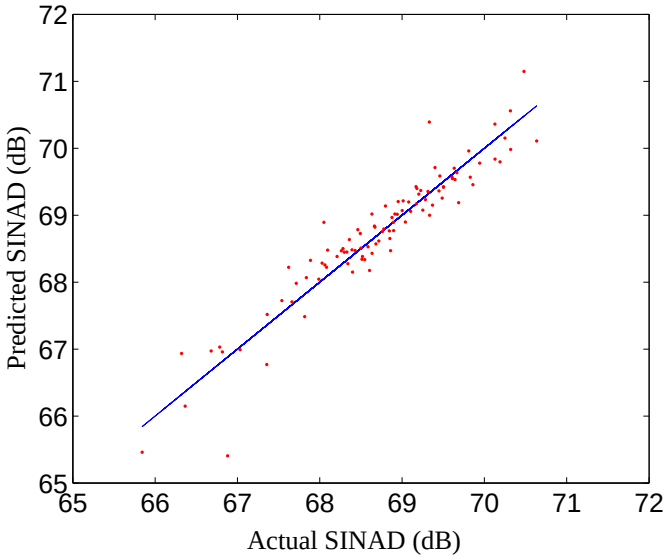


(a) Actual and Predicted ADC THD

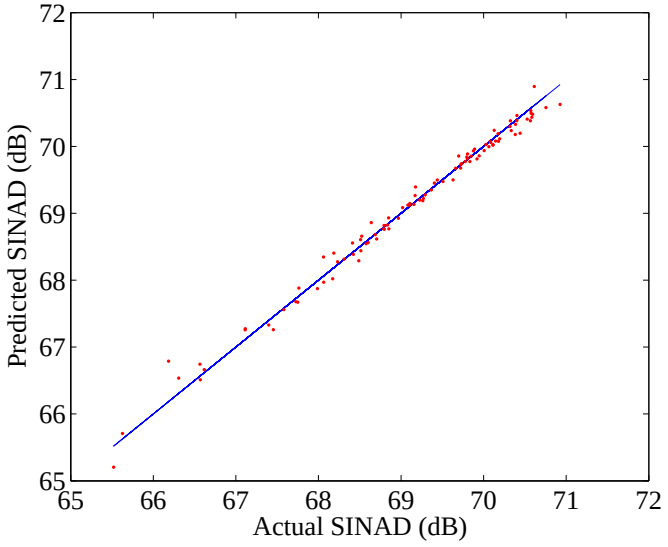


(b) Actual and Predicted DAC THD

Figure 4.8: Comparison of Actual and Predicted THD (Simulation Data)



(a) Actual and Predicted ADC SINAD



(b) Actual and Predicted DAC SINAD

Figure 4.9: Comparison of Actual and Predicted SINAD (Simulation Data)

Table 4.3: Prediction Errors with respect to Order of Filter

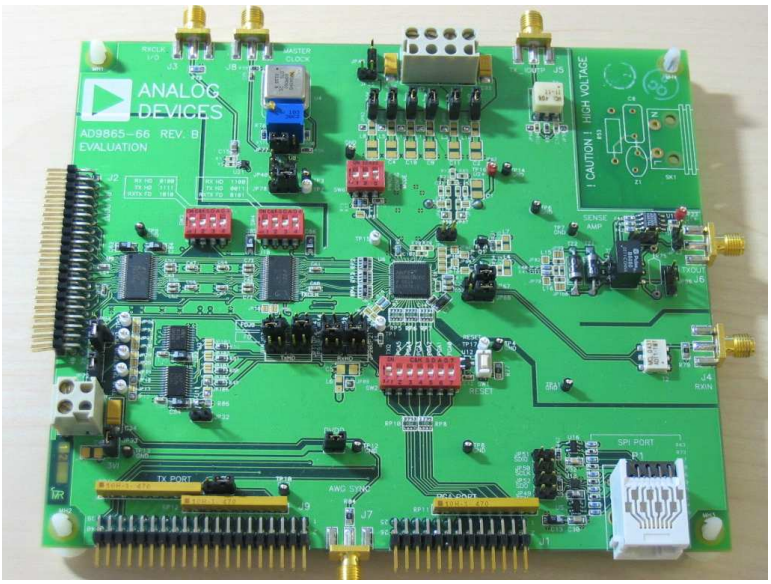
	DAC channel			
	THD		**SNR**	
	Mean	**STD.**	**Mean**	**STD.**
1st-order	0.07dB	0.07dB	0.85dB	0.71dB
2nd-order	0.07dB	0.07dB	0.81dB	0.68dB
3rd-order	0.08dB	0.15dB	0.91dB	0.90dB
	ADC channel			
	THD		**SNR**	
	Mean	**STD.**	**Mean**	**STD.**
1st-order	0.29dB	0.31dB	0.26dB	0.23dB
2nd-order	0.26dB	0.41dB	0.07dB	0.07dB
3rd-order	0.30dB	0.62dB	0.02dB	0.02dB

$fs/2$, the normal and filtered response make no difference each other. In the simulation setup described above, f_N is placed between the fundamental components of the first and second tone, so that -4dB difference between the amplitude of 5th harmonics components of the normal and filtered response was made. The order of the filter may determine the width of the transition band. In general, higher order filter shows more abrupt transition between the passband and the stopband, therefore it is desirable when the filter is used to eliminate non-ideal components from the signal. However, in this scheme, the filter should have reasonably a gradual transition in order not to lose the amplitude information of higher-order harmonics. In order to see the effects of the width of filter's transition band, loopback schemes with the filters of various orders were simulated. Table 4.3 shows the prediction errors

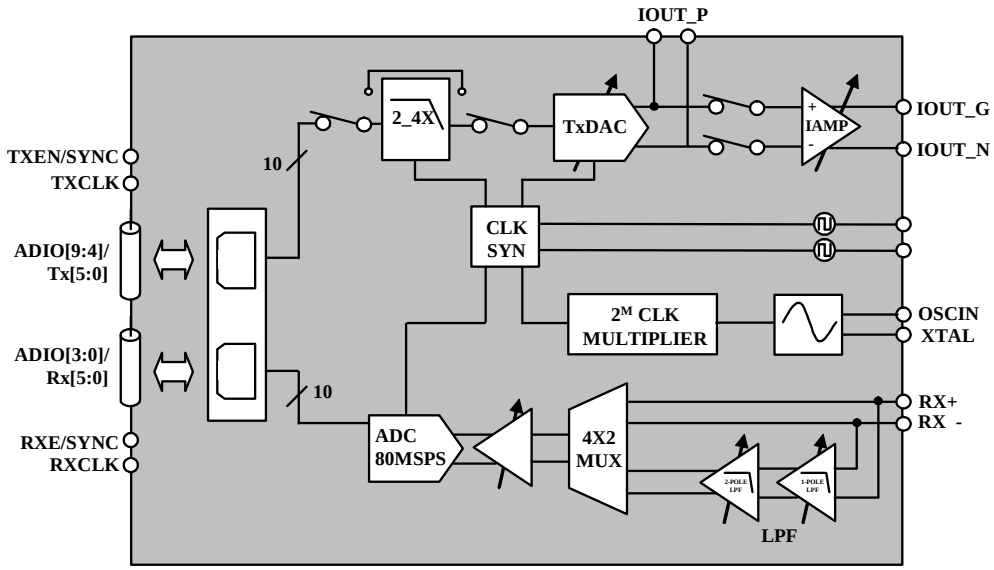
for the first to third order filters. In THD estimation of both DAC and ADC channel, the error slightly increases as the order of the filter increases. For SNR estimation of the ADC channel, the higher-order filter produced more accurate estimation. In contrast, the error increases in the DAC channel as the order of the filter increases.

4.4.2 Hardware Measurements

Hardware measurements were performed on a commercial broadband modem mixed-signal front-end IC (Analog Devices AD9865) [3], and its block diagram is shown in Figure 4.10. The AD9865 is a mixed-signal front end IC for transceiver application requiring Tx and Rx path functionality with data rates up to 80MSPS. The Tx signal path consists of a bypassable 2x/4x low-pass interpolation filter, a 10-bit TxDAC, and programmable gain driver. The gain of the Tx signal path can be configured by the TxDAC and the driver. The receive path is composed of a tunable 3-pole low-pass filter, a programmable gain amplifier, and a 10-bit ADC. The lowpass filter cutoff frequency can be set over a 15MHz to 35MHz range or simply bypassed. In this experiment, the filter was bypassed in normal functional mode, and turned on in a test mode, generating a weighted response to emulate the on-board filter in Figure 4.4. Unlike the simulation setup in the previous section, $Y_{\omega_0}(\omega)$ and $Y_{\omega_1}(\omega)$ in Equation 4.17 were generated separately.

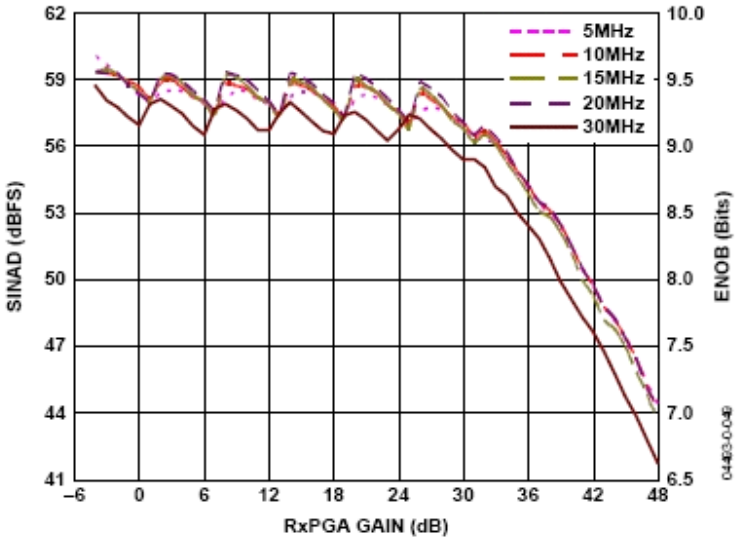


(a) AD9865

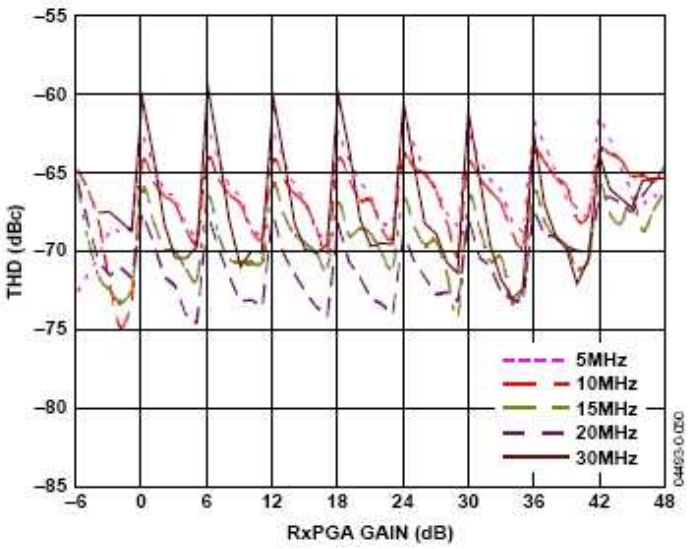


(b) AD9865 Block Diagram

Figure 4.10: AD9865 Block Diagram



(a) SINAD vs. RxPGA and Input Frequency



(b) THD vs. RxPGA and Input Frequency

Figure 4.11: SINAD and THD vs. RxPGA and Input Frequency

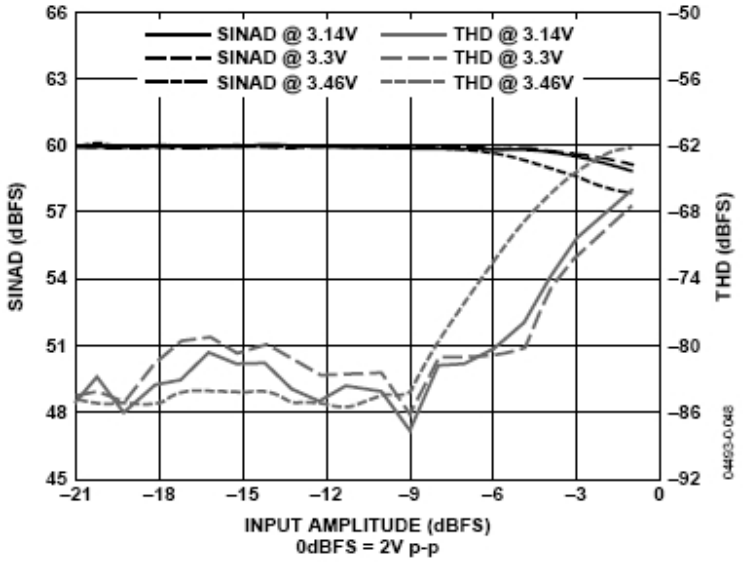


Figure 4.12: SINAD Vs. Input Amplitude and Supply Voltage

4.4.2.1 Fault Injection

In order to inject a fault in the AD9865, measurements were performed under various conditions by sweeping the power supplies, the input amplitude and re-configuring the Rx/Tx gain, and by combining them. Figure 4.11 shows the variations of the SINAD and THD of the AD 9865 with respect to different RxPGA gains and input frequencies, and Figure 4.12 shows the variations with respect to various input amplitudes and supply voltages. This result implies that the performance varies according to the input and environmental conditions. Firstly, the performance of Rx and Tx channels to various conditions were measured separately with an analog signal generator and measurement equipment. This results in 88 DUTs with 7dB of variations in THD, and 20dB

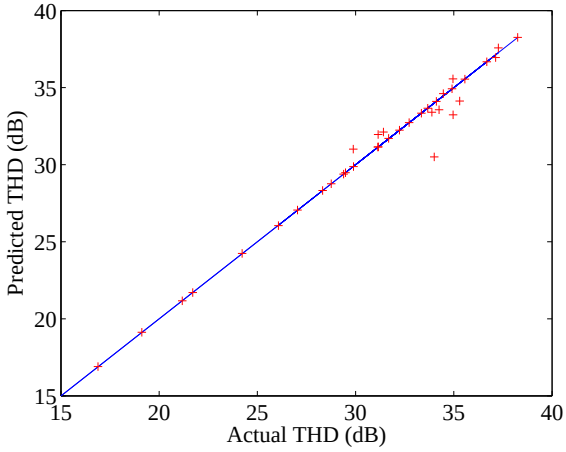
Table 4.4: Mean and Standard Deviation of Prediction Errors for Hardware Measurements

Parameter	**Tx channel**		**Rx channel**	
	Mean	**STD.**	**Mean**	**STD.**
SNR (dB)	0.32dB	0.67dB	1.35dB	2.43dB
THD (dB)	0.31dB	0.57dB	0.63dB	1.40dB
SINAD (dB)	0.25dB	0.41dB	0.94dB	1.57dB

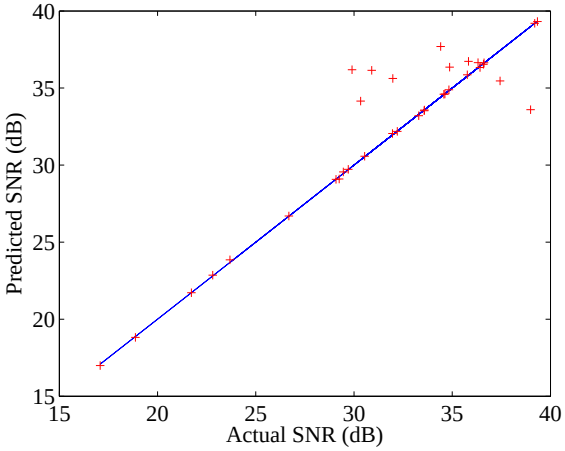
in SNR. Then, the loopback responses were measured, and the performance parameters of Tx and Rx channels were predicted using the spectral prediction technique. For the regression technique, 48 DUTs were used for the training set, and 40 DUTs were used for the validation.

4.4.2.2 Results

Figure 4.13 shows the predicted SNR for 40 validation DUTs. As in the simulation, the prediction errors of the Tx channel is higher than those of the Rx channel. In addition, the predicted versus the actual THD of 40 DUTs are plotted in Figure 4.14. It can be seen that more errors occurred in DUTs of higher THD. This is due to the fact that the distortion amplitude of higher THD is more likely to be varied or contaminated by the random noise. Table 4.4 summarizes the statistics of the prediction errors. As shown in Table 4.4, the prediction errors were within 2.4dB except for the SNR of the Tx channel. This is mainly due to one DUT which produced more than +10dB error in predicting the SNR of the Tx channel. Also, it shows that the prediction error was increased by approximately 1dB compared to the simulation results. This

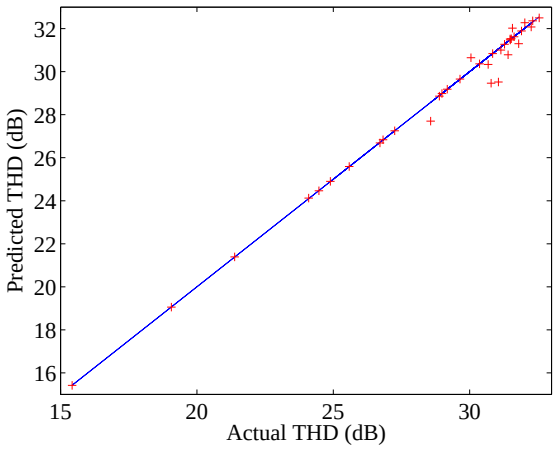


(a) Actual and Predicted ADC SNR

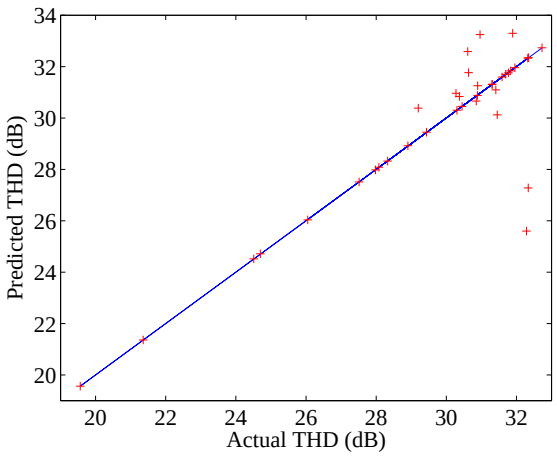


(b) Actual and Predicted DAC SNR

Figure 4.13: Comparison of Actual and Predicted SNR (Hardware measurements)

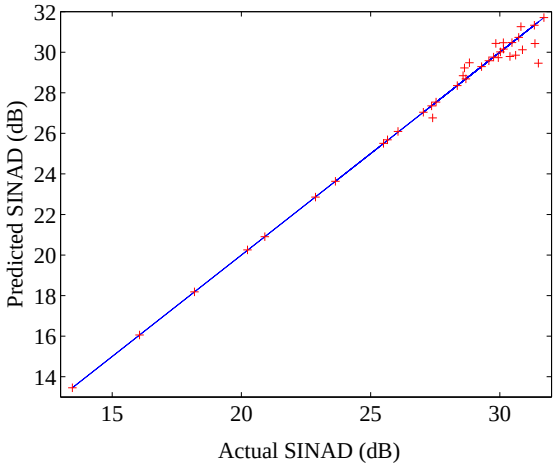


(a) Actual and Predicted ADC THD

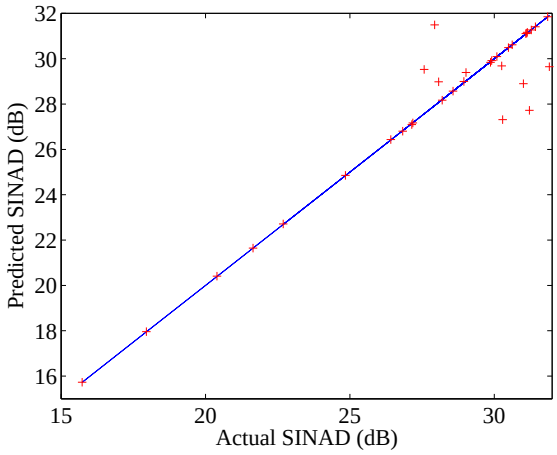


(b) Actual and Predicted DAC THD

Figure 4.14: Comparison of Actual and Predicted THD (Hardware measurements)



(a) Actual and Predicted ADC SINAD



(b) Actual and Predicted DAC SINAD

Figure 4.15: Comparison of Actual and Predicted SINAD (Hardware measurements)

is primarily due to the measurement error, which we observed to be $\pm 0.6dB$.

4.4.3 Summary

Loopback testing of Mixed-signal SOCs provides a low-cost test solution, but suffers from fault masking, resulting in serious yield loss and low test accuracy. This chapter presented an efficient loopback test methodology which enables individual characterization of dynamic performance of Devices Under Test (DUTs) in loopback mode. DUTs are loop-backed externally on the DIB, and a simple filter and an analog adder on the DIB produce a composite loopback response. Two test schemes were introduced, and each scheme was validated through either the hardware measurements or simulations. These experimental results show that the dynamic performance parameters of each channel were characterized accurately with a prediction error of 2.4dB. This test scheme can be readily implemented on a conventional loopback scheme with an external connection and a low-cost analog filter. It does not depend on the type of circuits, and thus can be applied to general mixed-signal circuits.

Chapter 5

A Statistical Digital Equalizer for Linearity Test of Embedded Data Converters

The use of uncalibrated on-chip analog circuits may not guarantee the quality of the analog signals generated or measured on a given DUT [14]. The spectral prediction technique discussed in the previous chapter has tackled this issue by characterizing the performance of the on-chip circuits individually and thereby separating the sources of the signal degradation. However, this strategy may not be sufficient in testing static linearity parameters as the linearity interaction between the tested circuits and the circuits for test tend to cancel, making the faults unobservable. Also, the loss of test accuracy due to this linearity interaction may occur when a low cost tester where the linearity specification may not exceed the requirements, is used. This chapter investigates BIST techniques to overcome this linearity interaction issue.

5.1 A Static Linearity Test

5.1.1 Comparison between Static and Dynamic Linearity Tests

As discussed in the previous chapter, Total Harmonic Distortion Test that determines the ratio of fundamental signal power to the power of its harmonics is also involved in a linearity measure of analog devices based on a

sine-wave model (Taylor Series). The key difference between static linearity and dynamic linearity (i.e. THD) is a domain that DUTs are evaluated. In dynamic linearity test, the frequency response to a single tone or multi-tone signal whose fundamental frequencies are within its functional bands is evaluated. In contrast, the voltage or current amplitude response to DC or almost DC-like slow signal is used to estimate the behavior of a DUT in static linearity test.

The focus of linearity testing of data converters varies from case to case [40]. For communication applications, a device is often characterized by dynamic linearity behavior. On the other hand, for high-resolution imaging/video applications, the uniformity of the step sizes between codes (Differential NonLinearity) and the deviation of actual Code Transition (CT) levels from the ideal transition levels (Integral NonLinearity) are key parameters which represent static linearity. While a typical linearity testing for communication applications requires a few thousand samples [33], Integral NonLinearity (INL) and Differential NonLinearity (DNL) testing involve the measurement of all $2^n - 1$ CTs (n is the number of bits of the device), which usually requires much larger samples and longer test time because every code must be tested several times at very low speed. Therefore, it is obvious that linearity tests such as INL and DNL are highly time-consuming and expensive [20].

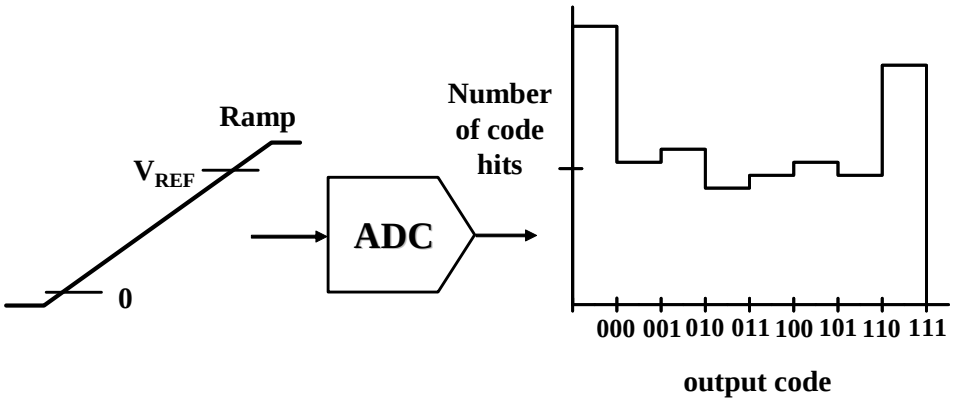


Figure 5.1: A Test Setup for A Standard Histogram-based Test

5.1.2 A Standard Histogram-based Testing

A well-known test method for INL and DNL is a histogram test [14, 40]. In a histogram test, a linear ramp or sine signal is applied to a DUT and the number of occurrences of each output code is plotted as a histogram. The number of occurrences of the output code is directly proportional to the width of the code. In other words, wide codes are hit more often than narrow codes. Figure 5.1 shows a simplified block diagram of an ADC histogram test setup. The ith code width $CW(i)$ can be calculated from the collected histogram in units of Least Significant Bits (LSBs) using the following equation.

$$CW(i) = \frac{count(i)}{\frac{1}{2^N-2}\sum_{k=1}^{2^N-2} count(k)}, \quad i = 1, 2, \ldots, 2^N - 2 \tag{5.1}$$

where $count(i)$ is the number of hits that occurs for ith code, and the highest and lowest code width are excluded as the widths are infinite. DNL in units of LSBs can be determined by subtracting one LSB from each code width as

follows.

$$DNL(i) = CW(i) - 1, \quad i = 1, 2, \ldots, 2^N - 2 \tag{5.2}$$

By integrating the DNLs, INL can be determined from the following equation.

$$INL(i) = \sum_{k=1}^{i} DNL(k), \quad i = 1, 2, \ldots, 2^N - 2 \tag{5.3}$$

It is important to note that in order for Equation 5.1 to be valid, a perfectly linear ramp is used as a test input. Otherwise, $CW(i)$ will be corrupted by the non-linearity of the test input.

5.1.3 Statistical Nature of Histogram-based Test

As analog and mixed-signal circuits in data converters generate random noise, the DUT in Figure 5.1 can be modeled as a combination of a perfect DUT and a random noise source [14, 73]. When the noise source is placed prior to the DUT, it is called *input referred noise* and *output referred noise* in the opposite case. To understand noisy behavior of data converters, consider a noisy DAC with a DC input voltage as shown in Figure 5.2. The noisy DAC is modeled as a combination of noise-free DAC and a Gaussian noise source whose the mean is zero and the standard deviation is σ. If σ is zero, then the DAC will always produce the same analog signal. However, due to the noise voltage, the analog output voltage of the DAC is randomly dithered with noise, resulting in uncertainty in the output response. We can model the outcome of the noisy DAC as a random signal whose Probability Density Function (*pdf*) has the same form as the *pdf* of the noise source, but the mean

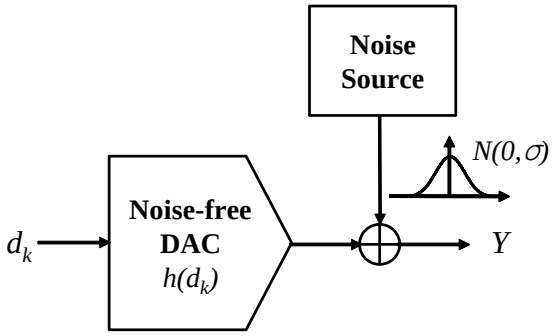


Figure 5.2: Statistical Behavior of Noisy DACs

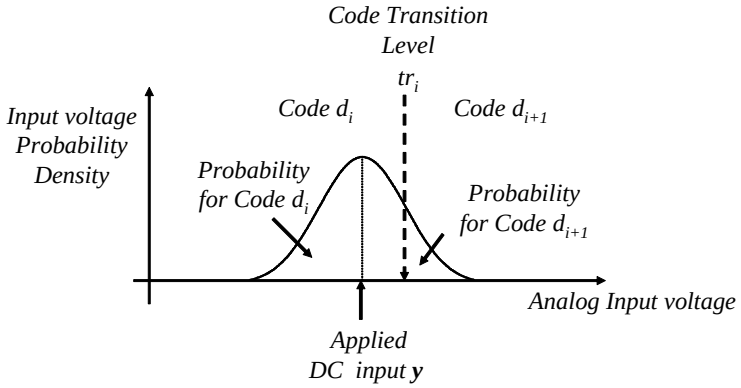


Figure 5.3: Probability Density Plot for an Analog Input to noisy ADC

value is different.

$$f_Y(y) = \frac{1}{\sqrt{2\pi}\sigma} e^{-(y-h(d_k))^2/2\sigma^2} \tag{5.4}$$

where Y is the outcome of the DAC to input DC voltage d_k and $f_Y(y)$ is pdf of Y, and $h(\cdot)$ is the deterministic transfer function of the DAC and $h(d_k)$ is the output of the noise-free DAC (σ is zero). Also, the behavior of noisy ADCs can be modeled with the similar way as the noisy DACs. However, unlike the DAC with output referred noise source, the ADC is often modeled

with input referred noise source, and the outcome is typically described by the probability that the code will occur at the given analog input voltage. As shown in Figure 5.3, the applied DC analog input is dithered due to the noise, and the dithered analog voltage which exceeds the code transition voltage (tr_i) will be converted into the digital code d_{i+1}. The probability that the input voltage will be converted into the digital code d_i is equal to the area underneath the portion of the analog input voltage pdf that is between tr_{i-1} and tr_i.

$$P(d_i) = \frac{1}{\sqrt{2\pi}\sigma} \int_{tr_{i-1}}^{tr_i} e^{-(s-y)^2/2\sigma^2} ds \tag{5.5}$$

If the DC input voltage is exactly equal to a transition level (i.e. $y = tr_i$, then the area under the pdf is equally split between code d_i and d_{i+1}, and the code d_i and d_{i+1} will be produced with the equal probability.

5.1.4 Test condition for Accurate Static Linearity Test

The noise introduced by inherent device noise or measurement instruments may produce an erroneous conversion result. In order to avoid such errors in the histogram test, it is important to obtain sufficient number of samples and decide the code width $CW(i)$ with high confidence interval. Hence, in a practical test, each code must be excited several times with highly linear inputs to ensure uniform hit probability of each code when each code is ideally spaced.

5.2 Limitations of Loopback-based Technique for Static Linearity Test

For the system which includes both ADCs and DACs, a loopback scheme can be used for the static linearity testing of the ADCs and DACs by looping back the analog DAC output into the input of the ADC [22, 80]. This method, however, suffers from fault masking (INL Error Masking), leading to serious yield loss and low test accuracy. In particular, unlike dynamic parameter testing where noise and distortion parameters are additive, static parameters such as INL and DNL tend to cancel, making standard test approaches such as a histogram-based method impractical. In the following section, INL error masking issue which makes loopback-based static linearity test impractical is investigated.

5.2.1 INL Error Masking

In order to better understand fault masking issue in loopback tests, consider an N-bit ADC and DAC in a loopback mode as shown in Figure 5.4. The INL and DNL of the ADC are being tested with analog input y generated by the DAC. Here, the DAC and ADC are modeled as a combination of noise-free ADC and DAC, and a Gaussian noise source whose the standard deviation is σ [14, 73]. As discussed previously, due to this statistical behavior, the analog input y can be represented as a random signal. Suppose each code of the DAC is excited to generate a ramp to the ADC, then the Cumulative Distribution

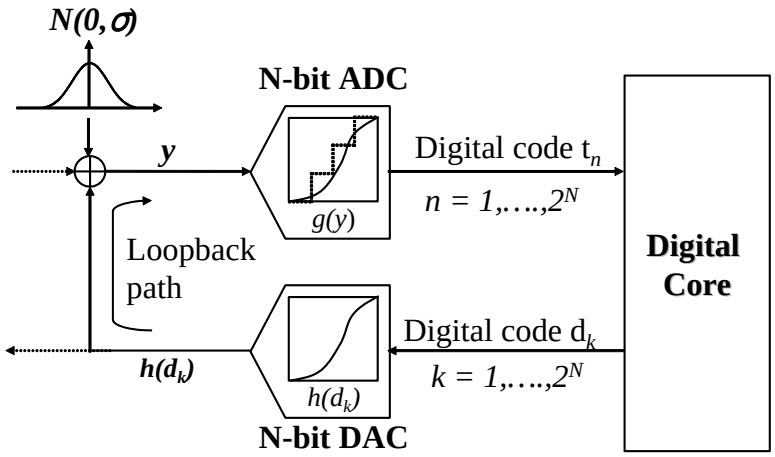


Figure 5.4: A Setup for a Conventional Loopback-based Test

Function (CDF) of analog input y can be written as follows.

$$F_Y(y) = \frac{1}{2^N} \sum_{k=1}^{2^N} \Phi\left(\frac{y - h(d_k)}{\sigma}\right) \tag{5.6}$$

where $h(d_k)$ is the transfer function of the DAC which determines the corresponding analog output for a given digital code d_k. For simplicity, we assume that 1 LSB is 1V. $\Phi(y)$ is the CDF for the Gaussian noise with mean zero and standard deviation one.

If the DAC is ideal, i.e., $h(d_k) = k$ for all $k = 1, \ldots, 2^N$, then Equation 5.6 can be re-written as

$$F_Y(y) = \frac{1}{2^N} \sum_{k=1}^{2^N} \Phi\left(\frac{y - k}{\sigma}\right) \tag{5.7}$$

and the probability of $m - 1 < y \leq m$ for $1 < m < 2^N$ can be calculated by

subtracting $F_Y(m-1)$ from $F_Y(m)$ as follows.

$$\begin{aligned} F_Y(m) - F_Y(m-1) =& \frac{1}{2^N}\sum_{k=1}^{2^N}\Phi\left(\frac{m-k}{\sigma}\right) - \frac{1}{2^N}\sum_{k=1}^{2^N}\Phi\left(\frac{m-1-k}{\sigma}\right) \\ =& \frac{1}{2^N}\left(\Phi\left(\frac{m-1}{\sigma}\right) - \Phi\left(\frac{m-1-2^N}{\sigma}\right)\right) \end{aligned} \tag{5.8}$$

Therefore, if m is sufficiently larger than $h(d_1)$ and smaller than $h(d_{2^N})$, i.e., $3\sigma \ll \|m-1\|$ and $3\sigma \ll \|2^N - 1 - m\|$, then

$$\Phi\left(\frac{m-1}{\sigma}\right) \approx 1 \quad \text{for} \quad m-1 \gg 3\sigma \tag{5.9}$$

and

$$\Phi\left(\frac{m-1-2^N}{\sigma}\right) \approx 0 \quad \text{for} \quad m-2^N-1 \ll -3\sigma \tag{5.10}$$

and thus $F_Y(m) - F_Y(m-1)$ becomes $\frac{1}{2^N}$. Figure 5.5 shows the input voltage probability generated by a perfectly linear and noisy DAC. The ideal DAC produces analog outputs whose average voltages are equally spaced and the noise is superimposed on the average voltages. As can be seen in this Figure, the area of intervals of 1 LSB are equal, resulting in the probabilities of 1 LSB intervals are equal over the ranges specified above. The reason that this is valid for certain ranges is the analog signal which is closed to LSB and MSB may not be symmetrically dithered. Equation 5.1 can thus be used confidently to estimate INLs and DNLs of the ADC as the uniform distribution of analog input y is ensured in 1 LSB interval as long as $h(d_k)$ of the DAC is ideal.

However, the non-linearity of $h(d_k)$ may cause a significant impact on the accuracy of the code width calculation in Equation 5.1. Now suppose

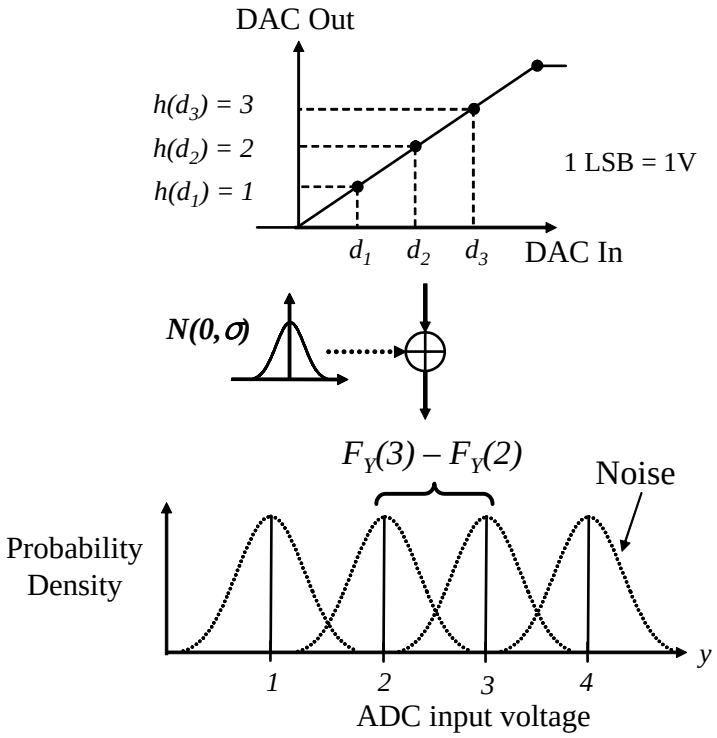


Figure 5.5: Input Voltage Probability Density Generated by a Perfectly Linear DAC

$h(d_j)$ of the code d_j is deviated from its ideal value by the error ε such that $j - h(d_j) = \varepsilon$. We can re-write Equation 5.8 as follows.

$$F_Y(m) - F_Y(m-1) = \frac{1}{2^N} + \frac{1}{2^N}\alpha \tag{5.11}$$

where

$$\alpha = \frac{1}{\sqrt{2\pi}\sigma} \int_0^{\varepsilon} \left(e^{-(x-(j-m))^2/2\sigma^2} - e^{-(x-(j+1-m))^2/2\sigma^2} \right) dx \tag{5.12}$$

The α in Equation 5.11 is due to the INL error of $h(d_j)$. If ε is positive and $j < m$, α is positive so that more samples hit the codes of the ADC which fall between m and $m-1$ and vice versa. Figure 5.6 illustrates non-uniform probability density of the ADC analog input voltage due to non-linearity of the DAC.

In summary, the errors in $h(d_k)$ may mask the DNL and INL errors of the ADC, because the number of code occurrences which is directly used to determine the code width, is also a function of non-linearity of the DAC. Thus it may contaminate the test results of the conventional histogram method. In the following sections, a new Built-in Self Test (BIST) method based on efficient digital equalization and spectral prediction techniques is discussed.

5.3 Static Linearity Test based on a Statistical Digital Equalizer

5.3.1 BIST scheme for Static Linearity Test

Figure 5.7 shows the loopback test setup of the statistical digital equalization technique. The digital equalizer is implemented using an available

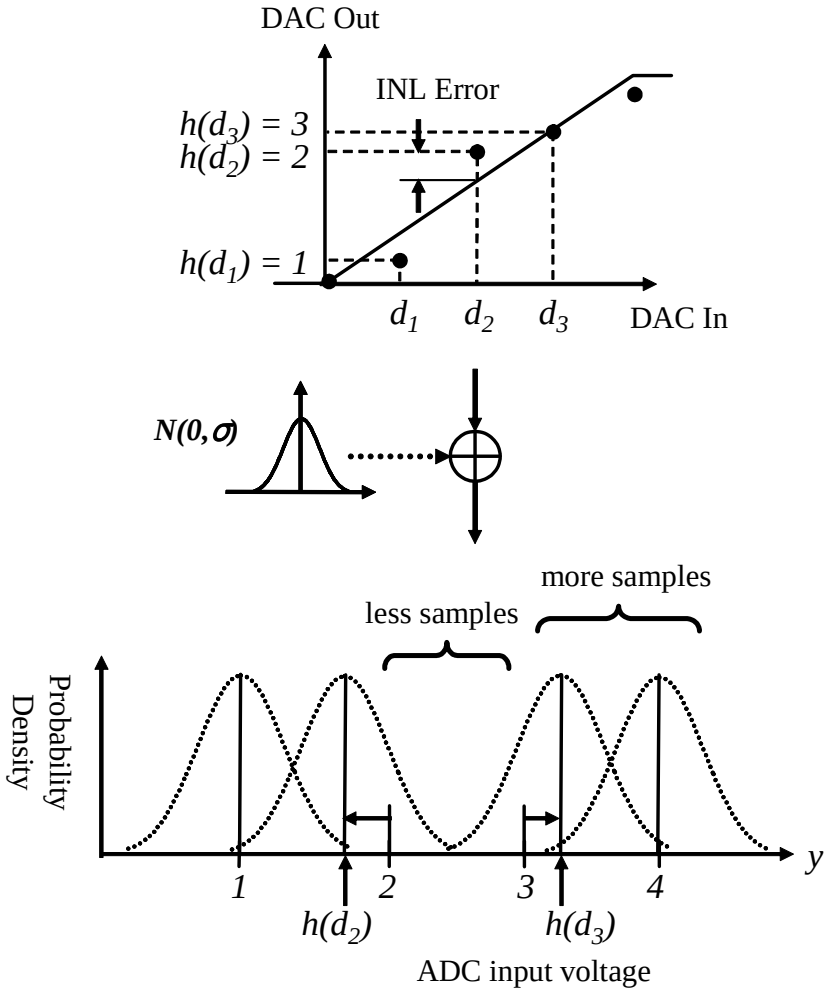


Figure 5.6: Comparison of Ramp Signals Generated by Linear and non-linear DAC

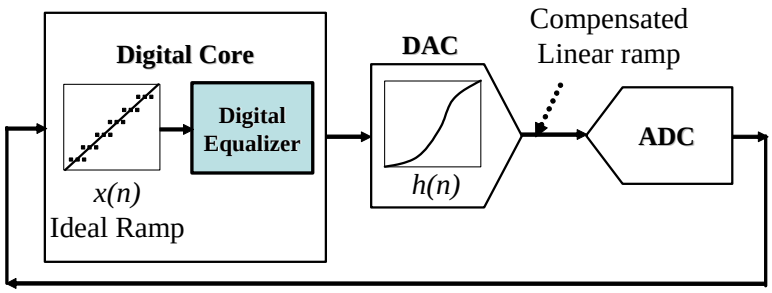


Figure 5.7: Loopback Test Setup underlying Proposed Approach

on-chip digital core. It generates digital codes in which INL errors of the DAC are compensated, and consequently the DAC can provide linear analog inputs to the ADC. A conventional histogram test is used to determine INLs and DNLs of the ADC based on the collected digital codes from the loopback response. The static parameters of the DAC can be re-calculated with the estimated INLs and DNLs of the ADC.

However, in practical systems, the transfer function of the DAC is not known with sufficient precision to allow for the accurate estimation of its inverse function. In addition, a naive compensation technique using the inverse transfer function has certain limitations in achieving the required linearity as the test stimulus of the histogram test. The following sections will discuss how we can estimate the transfer function of the DAC, and how we can design the compensation function which can provide highly linear test inputs to the ADC in a loopback mode.

5.3.2 Estimation of DAC Transfer Function

In Chapter 4, the loopback test methodology using the spectral prediction technique was presented. This method characterizes the nonlinearity of a device by estimating the power of harmonic contents of the output signal. From the estimated harmonic coefficients, the transfer function of DACs can be estimated using Chebyshev polynomials. The basic principle of Chebyshev polynomials is that when the transfer function of data converters can be represented as nth-order polynomials, it can be accurately estimated by the weighted sum of Chebyshev polynomials whose coefficients are harmonic coefficients of a single tone response [6, 23]. The estimated transfer function can be written as follows.

$$\tilde{h}(x) = \frac{\alpha_0}{2} + \sum_{k=1}^{n} \alpha_k C_k \left(\frac{x - A}{V} \right) \tag{5.13}$$

where α_k is kth harmonic coefficients for an applied single tone input $Vcos(\omega t)+A$ and C_k is the Chebyshev polynomials of the first kind. Chebyshev polynomials were previously used to estimate the transfer function of ADCs [6, 23], and its use is extended to DACs.

5.3.3 Statistical Digital Equalizer Design

A straightforward compensation for nonlinearity of data converters is to subtract its inverse distortion from the output signal [7, 47]. However, this compensation approach may not be sufficient to achieve the required linearity condition as a test stimulus of the histogram-based method. In fact, this

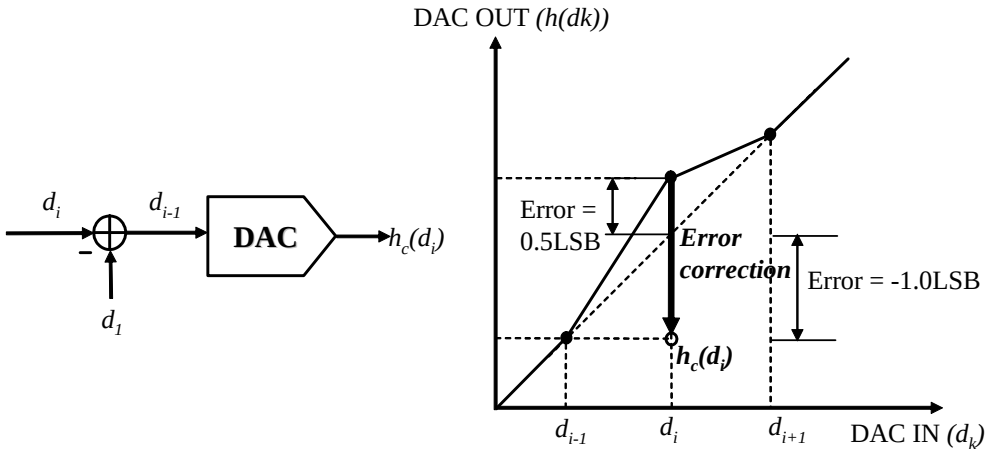


Figure 5.8: Example of Limitations of Naive Compensation

method is effective only when INL error is much larger than 1 LSB. Consider a nonlinear DAC whose $h(d_k)$ is the analog output for the digital code d_k where the INL error of d_{i-1} is zero, but d_i has +0.5 LSB INL error as shown in Figure 5.8. As switching d_i to d_{i-1} in order to compensate for a positive INL error, causes -1.0 LSB error, which is worse than the error prior to the compensation, the 0.5 LSB error cannot be compensated. Therefore, this approach may not be appropriate for the histogram-based test which requires higher linearity.

The equalization technique focuses on the linearization of a test stimulus which is used in the histogram-based test rather than a functional input in normal mode. As discussed earlier, in the histogram-based method, the codes are excited several times to overcome statistical non-idealities such as noise. In this method, by adjusting the number of samples per code effectively, the

cumulative probability of the analog output voltage which is generated from a nonlinear DAC, is linearized. The ADC can thus be tested with a linear test input which is actually non-linear, but guarantees uniform probability of hits for each code of the ADC under test.

Equation 5.7 can be re-written with weight factors which adjust the number of samples for each code.

$$F_Y(y) = \sum_{k=1}^{2^N} w_k \Phi\left(\frac{y - h(d_k)}{\sigma}\right) \tag{5.14}$$

where w_k is the weight factors for code d_k $(k = 1, \ldots, 2^N)$ and $\sum_{k=1}^{2^N} w_k = 1$. The goal is to find optimal weight factors which produce uniform probability of hits for each code of the ADC under test when the transfer function of the DAC is given. We can formulate this problem with Equation 5.14 as follows.

$$\text{argmin}_{\mathbf{w}=\{w_1,\ldots,w_{2^N}\}}(f(\mathbf{w})) \tag{5.15}$$

where

$$f(\mathbf{w}) = \sum_{i=2}^{2^N} \|F_Y(i) - F_Y(i-1) - \frac{1}{2^N}\|^2 \tag{5.16}$$

and

$$F_Y(y) = \sum_{k=1}^{2^N} w_k \Phi\left(\frac{y - h(d_k)}{\sigma}\right) \tag{5.17}$$

The example for weight factors is illustrated in Figure 5.9. As shown in this figure, w_2 is scaled down to avoid excessive hits between 1V and 2V of the ADC input. In contrast, w_3 is scaled up to compensate for sparse occurrences between 2V and 3V.

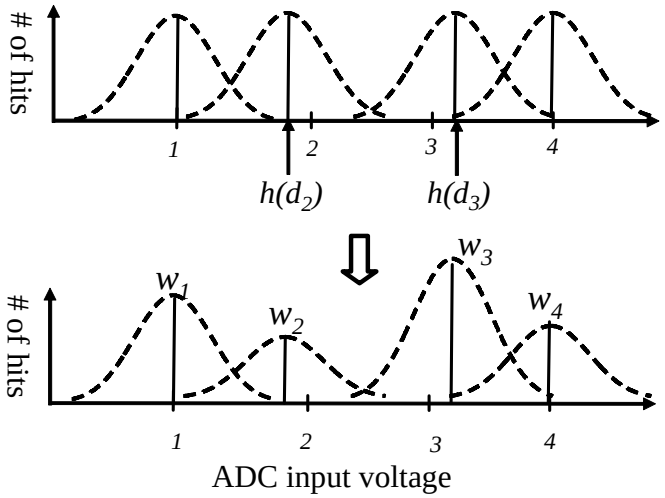


Figure 5.9: Example of Weight Factors

The computation of optimal weight factors may require considerable time overhead as it involves 2^N parameters and the sum of squares of 2^N non-linear functions. In a practical design, σ, which is the standard deviation of the noise, is less than a few LSBs. Therefore, if $h(d_k)$ is sufficiently smaller than y, then

$$w_k \Phi \left(\frac{y - h(d_k)}{\sigma} \right) = w_k \tag{5.18}$$

Also, in contrast, if $h(d_k)$ is sufficiently larger than y, then

$$w_k \Phi \left(\frac{y - h(d_k)}{\sigma} \right) \approx 0 \tag{5.19}$$

Equation 5.17 can thus be approximated as

$$\begin{aligned} F_Y(y) &= \sum_{k=1}^{y-\theta-1} w_k \Phi\left(\frac{y-h(d_k)}{\sigma}\right) + \sum_{k=y-\theta}^{y+\theta} w_k \Phi\left(\frac{y-h(d_k)}{\sigma}\right) \\ &\quad + \sum_{k=y-\theta+1}^{2^N} w_k \Phi\left(\frac{y-h(d_k)}{\sigma}\right) \\ &\approx \sum_{k=1}^{y-\theta-1} w_k + \sum_{k=y-\theta}^{y+\theta} w_k \Phi\left(\frac{y-h(d_k)}{\sigma}\right) \end{aligned} \tag{5.20}$$

where θ is the threshold limit of neighboring codes which are considered for the computation of $F_Y(y)$. θ can be chosen to be $\theta \gg \sigma$.

Based on this idea, we can further simplify the objective function $f(\mathbf{w})$ by dividing the optimization problem into several sub-problems. For instance, $f(\mathbf{w})$ can be decomposed into L sub-objective functions denoted as $f^{(1)}(\mathbf{w}^{(1)}), f^{(2)}(\mathbf{w}^{(2)}), \ldots, f^{(L)}(\mathbf{w}^{(L)})$. Each sub-objective function $f^{(l)}(\mathbf{w}^{(l)})$ contains M optimization variables.

$$f^{(l)}(\mathbf{w}^{(l)}) = \sum_{i=2}^{M} \| F_Y^{(l)}(i) - F_Y^{(l)}(i-1) - \frac{1}{M} \|^2 \tag{5.21}$$

where

$$\mathbf{w}^{(l)} = \{w_{(l-1)M+1}, w_{(l-1)M+2}, \ldots, w_{lM}\} \tag{5.22}$$

and

$$F_Y^{(l)}(y) = \sum_{k=1}^{M} w_k^{(l)} \Phi\left(\frac{y+(l-1)M-h(d_{k+(l-1)M})}{\sigma}\right) \tag{5.23}$$

It should be noted that the probabilities of $y \leq 1$ and $y > M$, i.e. $F_Y^{(l)}(1)$ and $1 - F_Y^{(l)}(M)$, are not included in Equation 5.21. Therefore, a naive combination of the obtained $w_k^{(l)}$ may result in errors as $F_Y^{(l)}(1)$ and $1 - F_Y^{(l)}(M)$

may affect $F_Y^{(l-1)}(y)$ and $F_Y^{(l+1)}(y)$. To avoid such errors, separate histograms are plotted for each $f^{(l)}(\mathbf{w}^{(l)})$ and the estimated DNLs are then combined to construct the INLs.

5.4 Simulation Results

The technique discussed in this section, was applied to 8-bit ADCs and DACs with MATLAB simulation. The reference voltage for both converters was set to 2V and 1 LSB was 0.0078V. The transfer functions of the ADCs and DACs were generated by introducing statistical variations with uniform distributions in the values of code widths (transition levels). Noisy ADCs and DACs were assumed, and the Gaussian noise source was modeled as shown in Figure 5.4. A ramp signal was used as a test stimulus; however this method can readily be extended with a sinusoidal signal.

This section is composed of two parts. The first part will discuss results for the estimation of DAC transfer function using the spectral prediction technique and Chebyshev polynomials. Subsequently, results for DNL and INL estimation of ADCs using the equalization technique will be presented.

5.4.1 Estimation of DAC Transfer Function Using Spectral Prediction Technique and Chebyshev Polynomials

As mentioned previously, the INL estimation technique is composed of two steps: the estimation of harmonic coefficients and the reconstruction of the transfer function of the DACs. Here it was assumed that the magnitudes of the

Table 5.1: INL and DNL Estimation Errors of DACs

	DAC Nonlinearity (LSB)				
	0.5	**1.0**	**2.0**	**3.0**	**4.0**
INL Est. Error (LSB)	0.12	0.32	0.37	0.67	1.06
DNL Est. Error (LSB)	0.05	0.11	0.15	0.23	0.28

Table 5.2: INL and DNL Estimation Errors with Ideal 8-bit DAC

INL Estimation Error	DNL Estimation Error
0.0525 LSB	0.0499 LSB

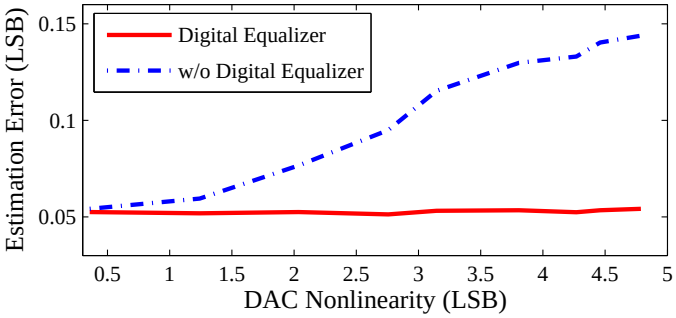
harmonic coefficients were given. Up to fifth order harmonics were considered. Table 5.1 summarizes the average value of prediction errors with respect to various nonlinearities of the DACs which are quantified as the maximum INL in units of LSBs. Unlike ADCs, the DNLs of the DACs were readily calculated with the obtained INL. The results indicate that the prediction error increase linearly as the nonlinearity of the DAC increases. This is due to the fact that a finite number of harmonics (5th-order) was observed. The inclusion of more harmonics in the Chebyshev polynomials may improve the prediction; however, this may require higher oversampling. In addition, the accuracy can be improved with the linearity test of the ADC which will be discussed in the following section.

5.4.2 DNL and INL Estimation of ADCs

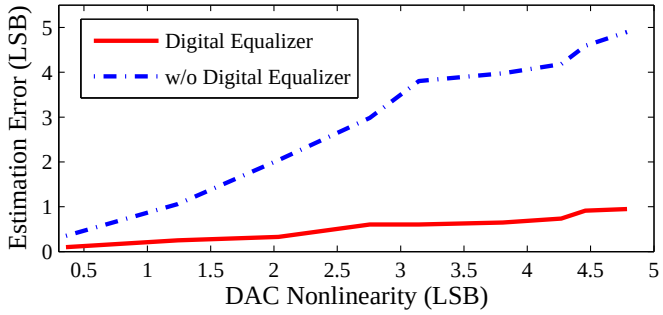
The DUTs with three different setups were simulated. The ADC was first simulated with an ideal quantized ramp generated by an ideal 8-bit DAC. The standard histogram test was then used to estimated INL and DNL. The results are summarized in Table 5.2. In addition, nonlinear DACs were placed in the loopback mode, and ramp signals were generated with both the conventional way and the digital equalization technique.

Figure 5.10 (a) and (b) show the estimation accuracy with respect to the DACs with various levels of performance. The results indicate that the conventional method suffers from the fault masking problem, and the estimation error sharply increases as the nonlinearity of the DACs increases. On the other hand, the method presented in this chapter is less sensitive to the fault masking problem. For the DACs with the maximum INL of 4.5 LSB, the prediction error was reduced by 80% compared to the conventional method. Therefore it can be inferred that the INL errors of the DACs can be compensated, thereby achieving accurate tests of the ADCs. The simulation results for various L values, which correspond to the number of sub-objective functions, are shown in Figure 5.10 (c). It can be seen that high accuracy can also be obtained with the optimization of several sub-objective functions. Figure 5.11 shows plots of the actual versus predicted INL and DNL of 2^8 codes.

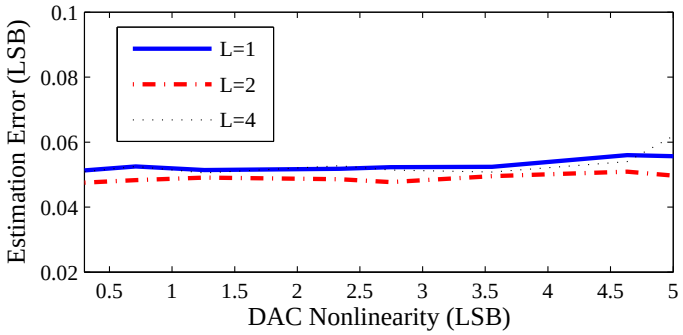
In addition, the sensitivity of the equalization technique to noise and the number of samples per code was simulated. The sensitivity to the number of samples per code is shown in Figure 5.12 (a). The results confirm that fault



(a) DNL Estimation Error of ADC



(b) INL Estimation Error of ADC



(c) Estimation Error with respect to L

Figure 5.10: Comparison of INL and DNL Prediction Errors Between Conventional and New Method

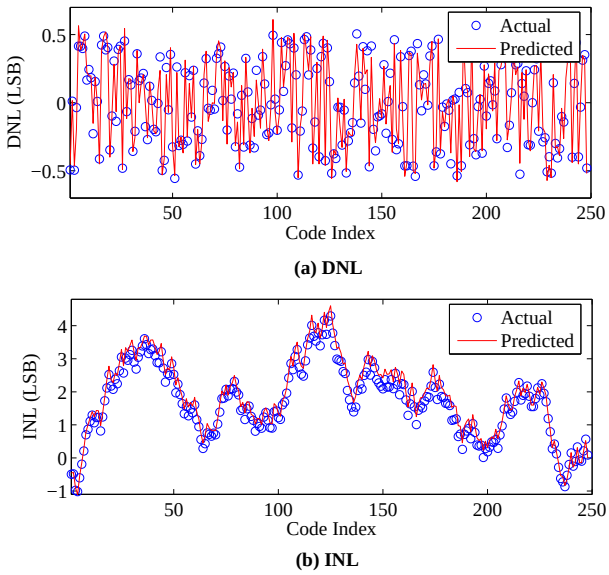


Figure 5.11: Comparison of Actual and Predicted INL and DNL

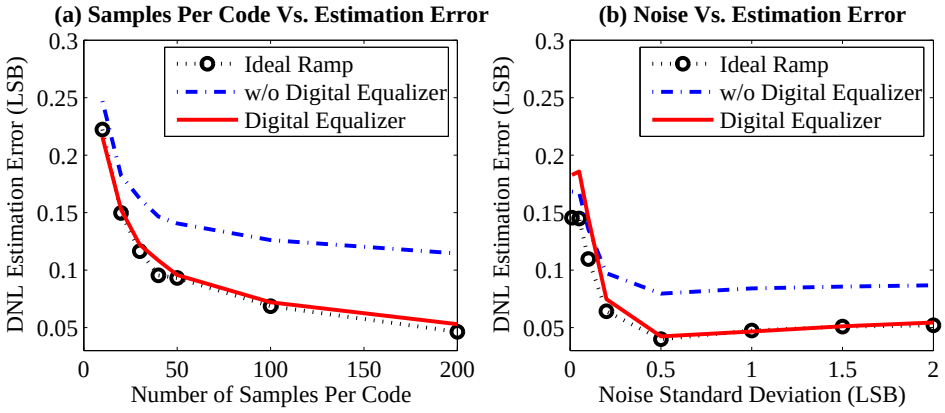


Figure 5.12: Prediction Error with respect to Samples per Code and Noise

masking may occur even in small samples. The accuracy can be improved with larger samples while it may not help much in the conventional method. Figure 5.12 (b) shows the DNL estimation errors for various amounts of injected noise whose magnitude is represented in units of LSBs. The results indicate that the accuracy of both the ideal test, assuming an ideal 8-bit DAC, and our method are low when the magnitude of the noise is smaller than 0.2 LSB. This is due to the finite number of discrete analog signals generated from the DACs with the finite resolution.

5.5 Summary

This chapter presented an efficient loopback-based linearity test technique using a digital equalizer. The digital equalizer compensates for the nonlinearity of a DAC by linearizing the cumulative probability of the analog output of the DAC which is randomly dithered with inherent noise. A standard histogram method can thus be used to test an ADC in a loopback mode with a statistically calibrated linear signal. The simulation results show that this method was as accurate as the case where an ideal ramp was assumed, and the estimation error was reduced by 80% compared to the conventional method, which suffers from the fault masking problem.

Chapter 6

Built-in Fault Diagnosis for Tunable Analog Systems Using an Ensemble Method

Efficient specification-oriented self test techniques has been elaborated thus far. These techniques accomplish a fast and economic test of embedded analog and mixed-signal cores by eliminating a traditional tester-based specification test. In addition, the test effectiveness is maintained by evaluating the performance of DUTs in a data sheet rather than a manipulated signature value. In this chapter, a fault diagnosis technique which re-uses the BIST techniques is investigated. The motivation here is to replace a time-consuming and expensive classical fault diagnosis with a new diagnosis procedure which utilizes a low-cost self-test.

6.1 Linear Error Modeling

This section provides a brief overview of a linear error model and sensitivity underlying most existing fault diagnosis methodologies [2, 67].

In a linear error model, the influence of deviation of device parameters on the performance parameters is linearized to simplify the problem. Consider an analog block with N circuit parameter c_i $(i = 1, \ldots, N)$, and a analog input

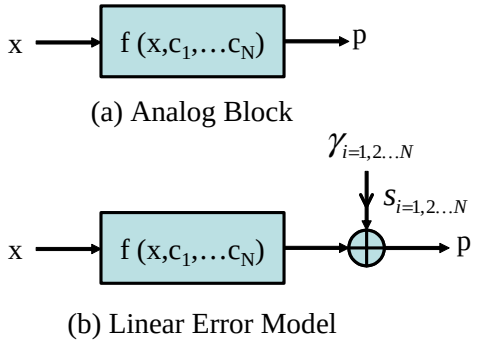


Figure 6.1: Analog Block and Linear Error Model

x is applied to this block as shown in Figure 6.1. The output measurement p can be expressed as

$$p = f(x, c_1, \ldots, c_N) = f(x, \underline{c}) \tag{6.1}$$

where $\underline{c}$ is the vector of c_i. A linear model can be used to approximate the output of analog blocks in which circuit parameters are perturbed with parameter variations $\underline{\gamma}$ [27, 65, 67]. The linearly approximated output p can be described by

$$p = f(x, \underline{c}) = f(x, (\underline{\dot{c}} + \underline{\gamma})) \cong f(x, \underline{\dot{c}}) + \sum_{i=1}^{N} s_i^p \gamma_i \tag{6.2}$$

where $\underline{\dot{c}}$ is the vector of nominal values of c_i and s_i^p is the sensitivity coefficients with respect to the output p, which is defined as

$$s_i^p = \left. \frac{\partial p}{\partial c_i} \right|_{\underline{\gamma}=0} \tag{6.3}$$

We can rewrite Equation 6.2 for many output measurements p_k $(k = 1, \ldots, M)$ in a matrix form as follows

$$\mathbf{P} = \dot{\mathbf{P}} + \mathbf{S\Gamma} \tag{6.4}$$

or

$$\begin{bmatrix} p_1 \\ p_2 \\ \vdots \\ p_M \end{bmatrix} = \begin{bmatrix} \dot{p}_1 \\ \dot{p}_2 \\ \vdots \\ \dot{p}_M \end{bmatrix} + \begin{bmatrix} s_1^{p_1} & s_2^{p_1} & \cdots & s_N^{p_1} \\ s_1^{p_2} & s_2^{p_2} & \cdots & s_N^{p_2} \\ \vdots & \vdots & \ddots & \vdots \\ s_1^{p_M} & s_2^{p_M} & \cdots & s_N^{p_M} \end{bmatrix} \begin{bmatrix} \gamma_1 \\ \gamma_2 \\ \vdots \\ \gamma_N \end{bmatrix}$$

where

$$\dot{\mathbf{P}} = \begin{bmatrix} \dot{p}_1 \\ \dot{p}_2 \\ \vdots \\ \dot{p}_M \end{bmatrix} \mathbf{S} = \begin{bmatrix} s_1^{p_1} & s_2^{p_1} & \cdots & s_N^{p_1} \\ s_1^{p_2} & s_2^{p_2} & \cdots & s_N^{p_2} \\ \vdots & \vdots & \ddots & \vdots \\ s_1^{p_M} & s_2^{p_M} & \cdots & s_N^{p_M} \end{bmatrix} \mathbf{\Gamma} = \begin{bmatrix} \gamma_1 \\ \gamma_2 \\ \vdots \\ \gamma_N \end{bmatrix}$$

and where $\dot{p}_k$ is the desired value of p_k. The sensitivity is often used to estimate the deviation of the circuit's performance to a change in the circuit. The optimization of sensitivity for a robust design is a crucial process in analog circuit design. Besides analog design, the sensitivity analysis and linear error modeling are also widely used in analog fault diagnosis [2, 32, 68, 76], As can be seen in Equation 6.4, the parameter variation $\underline{\gamma}$ can be determined by deriving the inverse matrix of $\mathbf{S}$. Due to the statistical nature of analog measurements, a linear Least Squares Estimate (LSE) [43] is often used. The LSE of Equation 6.4 can be expressed as

$$\hat{\mathbf{\Gamma}} = (\mathbf{S}^T\mathbf{S})^{-1}\mathbf{S}^T\mathbf{P} \tag{6.5}$$

where $\hat{\mathbf{\Gamma}}$ is the optimal LSE of $\mathbf{\Gamma}$.

6.2 BIST-based Analog Fault Diagnosis

A classical approach to solve Equation 6.5 is based on the observation of output responses to a set of functional inputs. This approach is, however,

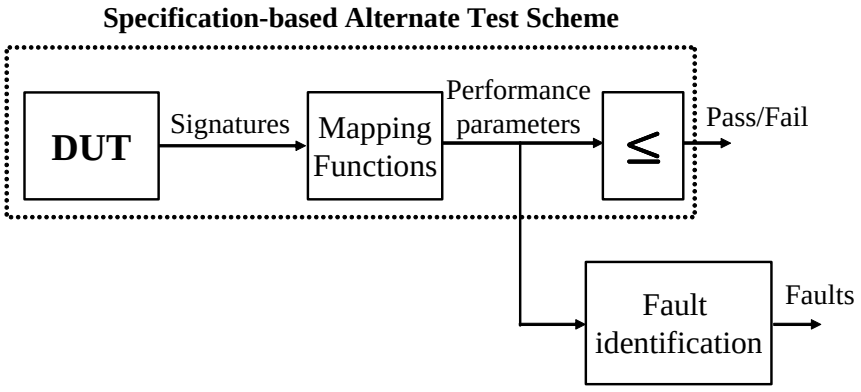


Figure 6.2: BIST-based Fault Diagnosis Scheme

quite expensive since we must measure as many specifications as unknown variable. Meanwhile, the self-test techniques discussed in previous chapters give us to measure the performance parameter indirectly with the signature values (time-encoded signature and spectral predictors) in a fast and cost-effective fashion. This implies that if such accurate built-in characterization tools are already available on-chip, then we can exploit such techniques to facilitate the fault diagnosis procedure.

This motivates the fault diagnosis scheme presented in this chapter. The fault diagnosis scheme relies on the specification-based BIST to generate the performance parameters, and they are used as measurements $\mathbf{P}$ to estimate $\mathbf{\Gamma}$ in Equation 6.5. Figure 6.2 shows a block diagram of the new fault diagnosis scheme based on BIST. The predicted performance parameters that are derived from the mapping function are used here for locating a fault. When a digital processor core is available on-chip, the scheme can be implemented with pure

on-chip hardware, as this method does not require external measurements. Obviously, this feature could facilitate both on-chip self-diagnosis and self-repair.

6.2.1 Limitations of BIST-based Analog Fault Diagnosis

This approach, however, may pose certain diagnosis limitations due to the limited capability and accuracy of the BIST. In other words, the obtained signatures may not be sufficient for the required diagnosis accuracy. For example, the number of the measurements M must be larger than or at least equal to the number of the unknown circuit parameters N so as for $(\mathbf{S}^T\mathbf{S})^{-1}$ in Equation 6.5 to exist [13]. The rank of $\mathbf{S}$ must be at least equal to the number of unknown variables. Otherwise, $(\mathbf{S}^T\mathbf{S})^{-1}$ becomes singular and not invertible. For large complex analog circuits, it may be difficult to achieve a sufficient number of measurements from on-chip BIST.

Furthermore, Chen et al. [16, 17] have shown that there exists dominance and equivalence between specifications. A specification has an acceptability region in a circuit parameter domain. A specification dominates another specification if the acceptability region of the former is fully enclosed and they are equivalent if matched. Due to these dominance and equivalence properties, the specifications do not always provide linearly independent measurements. To illustrate this, consider the sensitivity matrix below where the last two rows

dominate the first row.

$$\begin{bmatrix} p_1 \\ p_2 \\ p_3 \end{bmatrix} = \begin{bmatrix} 0.5 & 0.1 & 0.2 \\ 0.5 & 0 & 0 \\ 0 & 0.1 & 0.2 \end{bmatrix} \begin{bmatrix} s_1 \\ s_2 \\ s_3 \end{bmatrix}$$

In the following section, a novel diagnosability enhancement technique using parameter tuning will be discussed.

6.3 Diagnosability Enhancement using Parameter Tuning

The limited and imperfect measurements obtained from BIST may not provide accurate solutions in calculating the parameter variations from a linear error model. In the following sections, a new fault diagnosis technique using the supplemental signature obtained from a re-configured DUT is discussed. Firstly, the theory behind the supplemental signature is presented with the concept of high-order sensitivity, and then parameter tuning technique which effectively produces supplemental signature, is discussed. Finally, modified parameter variation equations which enable accurate identification of faults in a device, is presented.

6.3.1 Influence of Higher-Order Sensitivity

In Equation 6.3, the sensitivity coefficient $s_i^{p_k}$ is a single parameter sensitivity. In other words, the effects of variations of other circuit parameters are ignored, and $s_i^{p_k}$ is computed under the assumption that other circuit parameters are nominal.

However, in a real implementation, the values of the circuit parameters may vary in response to the variations of process parameters. In order to allow for influence of the variations of multiple circuit parameters, higher-order sensitivity coefficients should be considered. For example, the second-order sensitivity coefficients of c_i and c_j can be expressed as

$$s^{p_k}_{2,(i,j)} = \frac{1}{2}\frac{\partial^2 p_k}{\partial c_i \cdot \partial c_j}\bigg|_{\underline{\gamma}=0} \tag{6.6}$$

Thus, Equation 6.2 becomes

$$\begin{aligned} p_k &\cong f(x, \underline{\dot{c}}) + \delta \\ \delta &= \sum_{i=1}^{N} s^{p_k}_i \gamma_i + \sum_{j=1}^{N}\sum_{i=1}^{N} s^{p_k}_{2,(i,j)} \gamma_i \gamma_j \end{aligned} \tag{6.7}$$

Higher-order effects of sensitivity may be neglected during design optimization or catastrophic fault diagnosis. However, in a diagnosis phase whose accuracy strongly depends on the accuracy of the model, they may be considerable when the circuit parameters are under severe process variations and the magnitudes of higher-sensitivity coefficients are comparable to those of the linear-sensitivity coefficients.

In order to better understand the second-order effects of the sensitivity, consider an analog benchmark circuit shown in Figure 6.3. We simulate the benchmark circuit using Hspice, and compute the sensitivity of R_3 with respect to the performance parameters (gain and 3dB frequency) by changing the value of C_1. We assume that other circuit parameters have nominal values except for R_3 and C_1. Figure 6.4 shows the variations of sensitivity of R_3 to the

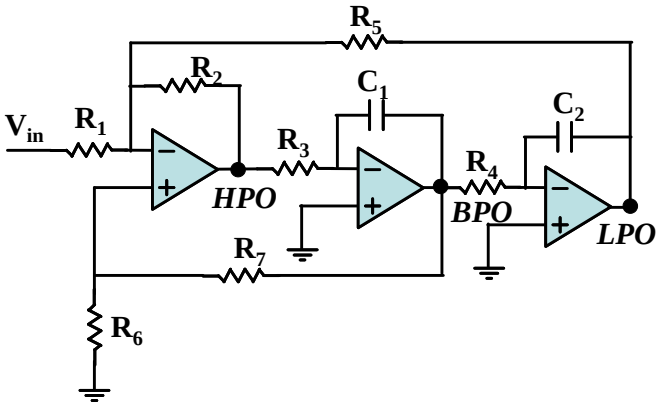
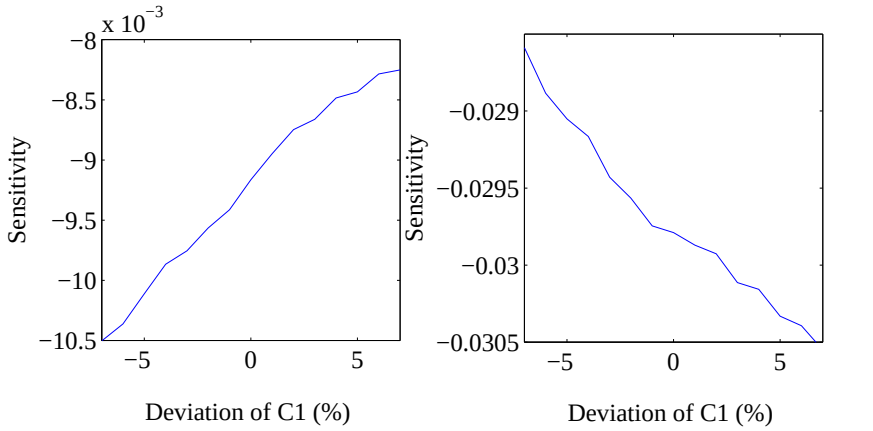


Figure 6.3: State-variable ITC Benchmark Circuit ($R_1 = R_2 = R_3 = R_4 = R_5 = 10\text{k}\Omega$, $R_6 = 3\text{k}\Omega$, $R_7 = 7\text{k}\Omega$, $C_1 = C_2 = 20\text{nf}$)



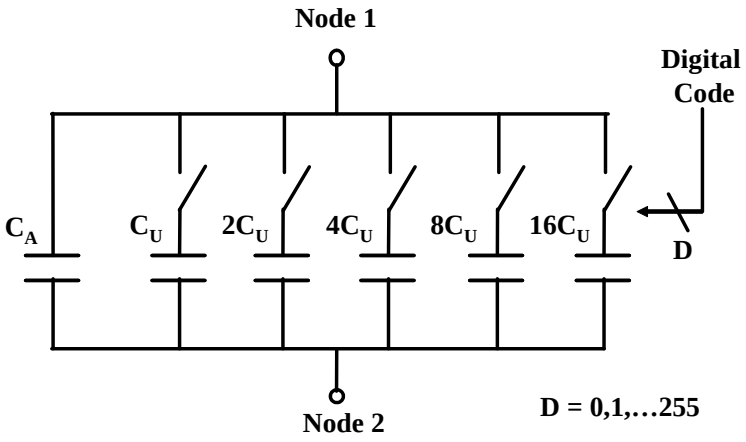
(a) Senstivity of R3 with respect to gain (b) Senstivity of R3 with respect to 3db

Figure 6.4: Sensitivity Deviations due to Second-order Effects

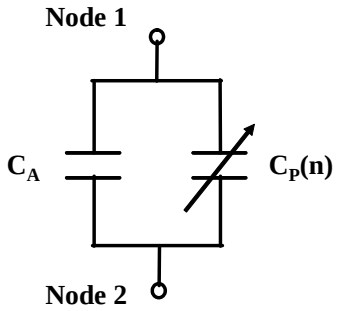
DC gain and 3dB frequency with respect to the variation of another circuit parameter C_1. The sensitivity of R_3 to DC gain increases as the value of C_1 increases. On the other hand, the sensitivity to 3dB frequency decreases. The slope corresponds to the second-order sensitivity $s_{2,(R_3,C_1)}$. Therefore, it can be inferred that due to the higher-order sensitivity, the changes of a parameter value may affect the sensitivity of other circuit parameters. It indicates that if we change the value of a circuit parameter on purpose, then we can obtain additional measurement $\mathbf{P}$ in Equation 6.4, which is a function of new sensitivities.

6.3.2 Parameter Tuning

Modern analog and mixed-signal devices have intelligent features which can interact with environmental fluctuations as well as manufacturing process variations. On-chip tuning which uses extra circuitry to adjust the performance parameters, is commonly used to achieve such features [21, 26, 30, 48, 72]. The extra circuitry is usually composed of replicas of some circuit components, and thus by controlling this extra circuitry, the functional parameter such as resistances, capacitances and transconductances can be adjusted. Programmable Capacitor Arrays (PCAs) and programmable resistors are commonly used for this purpose. Figure 6.5 shows an example for a typical PCA. The PCA can be realized as a fixed capacitor C_A in parallel with a n-bit binary weighted capacitor array. By switching the digital code, the actual capacitance between node 1 and node 2 varies. The unit capacitor C_u and the number of



(a) 5-bit Programmable Capacitor Array



(b) Equivalent Model

Figure 6.5: 5-bit Programmable Capacitor Array

bits depend on the tuning scheme, tuning resolution and range. So as to achieve fine tuning resolution, C_u must be sufficiently small, and similarly the bits of the binary weighted capacitor array must be large.

Here, programmability of a circuit parameter is exploited to obtain additional measurements from a DUT whose sensitivities are now different from those in a normal mode. In the following section, a new parameter variation estimation equation is derived, which takes into account this additional measurements.

6.3.3 Supplemental Parameter Variation Equation

Assume c_h is a programmable capacitor with n-bit PCA whose unit capacitor is C_u. ($c_h = C_A$ in Figure 6.5). For simplicity, further assume that the second-order sensitivity of other circuit parameters except for c_h is negligible, i.e., $s^{p_k}_{2,(i,j)} \cong 0$ for all $j \neq h$, then we can re-write δ in Equation 6.7 as follows.

$$\delta = \sum_{i=1}^{N} s_i^{p_k}\gamma_i + s_h^{p_k}C_P(n) + \sum_{i=1}^{N} s^{p_k}_{2,(i,h)}\gamma_i(\gamma_h + C_P(n)) \tag{6.8}$$

where $C_P(n)$ is the total capacitance of the programmable capacitor array in parallel with c_h when the digital control code is n. It has the form

$$C_P(n) = n \cdot C_u, \quad n = 0, 1, \cdots, 2^5 - 1 \tag{6.9}$$

$n = 0$ indicates that all switches in PCA are open and $C_P(0)$ is equal to C_A.

Equation 6.8 can be rearranged as follows

$$\begin{aligned}\delta &= \sum_{i=1}^{N}(s_i^{p_k} + s_{2,(i,h)}^{p_k}(\gamma_h + C_P(n)) \cdot \gamma_i + s_h^{p_k} C_P(n) \\ &= \sum_{i=1}^{N} a_i^{p_k}(n)\gamma_i + s_h^{p_k} C_P(n)\end{aligned} \tag{6.10}$$

where

$$a_i^{p_k}(n) = (s_i^{p_k} + s_{2,(i,h)}^{p_k} \cdot (\gamma_h + C_P(n))) \tag{6.11}$$

Here, $a_i^{p_k}(n)$ is new sensitivity coefficient of the circuit parameter c_i with respect to p_k for digital code n. It implies that the output measurement will change due to the change of the value of the programmable parameter and the altered sensitivities of other circuit parameters which are not tuned.

The representation of the output measurement in Equation 6.5 can be re-written with these additional measurements and altered sensitivities. For example, for 5-bit PCA, we can achieve an additional $2^5 - 1$ measurements and sensitivity matrix ($\mathbf{P}_n$ and $\mathbf{S}_n$, $n = 1, 2, \cdots, 2^5 - 1$). The new sensitivity matrix $\mathbf{S}_n$ can be expressed as follow $M \times N$ matrix.

$$\begin{aligned}\mathbf{S}_0 &= \begin{bmatrix} s_1^{p_1} & \cdots & s_N^{p_1} \\ \vdots & \ddots & \vdots \\ s_1^{p_M} & \cdots & s_N^{p_M} \end{bmatrix} \\ \mathbf{S}_n &= \begin{bmatrix} a_1^{p_1}(n) & \cdots & a_N^{p_1}(n) \\ \vdots & \ddots & \vdots \\ a_1^{p_M}(n) & \cdots & a_N^{p_M}(n) \end{bmatrix} \quad n = 1, \ldots, 2^5 - 1\end{aligned} \tag{6.12}$$

Finally, $(2^5 M) \times 1$ output measurement $\mathbf{P}_U$ can be expressed as

$$\mathbf{P_U} = \dot{\mathbf{P}}_\mathbf{U} + \mathbf{S_U}\boldsymbol{\Gamma} + \boldsymbol{\Theta} \tag{6.13}$$

where

$$\mathbf{S}_U = \begin{bmatrix} \mathbf{S}_0 \\ \mathbf{S}_1 \\ \vdots \\ \mathbf{S}_{31} \end{bmatrix}, \quad \mathbf{P}_U = \begin{bmatrix} \mathbf{P}_0 \\ \mathbf{P}_1 \\ \vdots \\ \mathbf{P}_{31} \end{bmatrix}, \quad \boldsymbol{\Gamma} = \begin{bmatrix} \gamma_1 \\ \gamma_2 \\ \vdots \\ \gamma_N \end{bmatrix} \tag{6.14}$$

and

$$\boldsymbol{\Theta} = \begin{bmatrix} \begin{bmatrix} 0 \\ \vdots \\ \vdots \end{bmatrix} \\ \begin{bmatrix} s_h^{p_1} C_p(0) \\ \vdots \\ s_h^{p_M} C_p(0) \end{bmatrix} \\ \vdots \\ \begin{bmatrix} s_h^{p_1} C_p(2^n - 1) \\ \vdots \\ s_h^{p_M} C_p(2^n - 1) \end{bmatrix} \end{bmatrix} \tag{6.15}$$

Also, we can express Equation 6.13 as

$$\begin{aligned} p_1 &= \dot{p}_1 + s_1^{p_1}\gamma_1 + \cdots + s_N^{p_1}\gamma_N \\ &\vdots \\ p_M &= \dot{p}_M + s_1^{p_M}\gamma_1 + \cdots + s_N^{p_M}\gamma_N \\ p_{M+1} &= \dot{p}_{M+1} + a_1^{p_{M+1}}(1)\gamma_1 + \cdots + a_N^{p_{M+1}}(1)\gamma_N + s_h^{p_1} C_P(1) \\ &\vdots \\ p_{32M} &= \dot{p}_{32M} + a_1^{p_{32M}}(31)\gamma_1 + \cdots + a_N^{p_{32M}}(31)\gamma_N + s_h^{p_M} C_P(31) \end{aligned} \tag{6.16}$$

In summary, the intended change of the tuning parameter as well as the resultant change of sensitivities of parameter variations vary the output of

the reconfigured DUT. Thereby, we can obtain different output measurements and the corresponding sensitivity matrix to estimate the parameter variations. Considering that typical tuning circuitry in a practical implementation uses 4-8 bit PCA, sufficient number of measurements can be achieved from on-chip BIST.

6.3.4 Implementation Flow

The major steps involved in fault diagnosis using the parameter tuning technique are depicted in Figure 6.6. The sensitivity coefficients of DUTs are obtained from the simulation for each tuning cycle, and the equations which describe parameter variations of DUT with the obtained sensitivity coefficients and performance parameters are derived. The circuit parameter variations are calculated by assigning the performance parameters measured from a real silicon into the obtained equations.

6.3.5 Issues

The intent of this section is to highlight some of the differences between the computations of the naive output parameter equation and the equation derived with the parameter tuning. First of all, as the matrix $\mathbf{S_U}$ is nonlinear with respect to $\mathbf{\Gamma}$ ($a_i^{p_k}(n)$ is nonlinear with respect to γ_i), Equation 6.16 should be solved by nonlinear approaches such as nonlinear least square estimates [44]. Secondly, since C_u also suffers from process variations and we are not able to identify its value unless it is tested separately, C_u must be treated as an

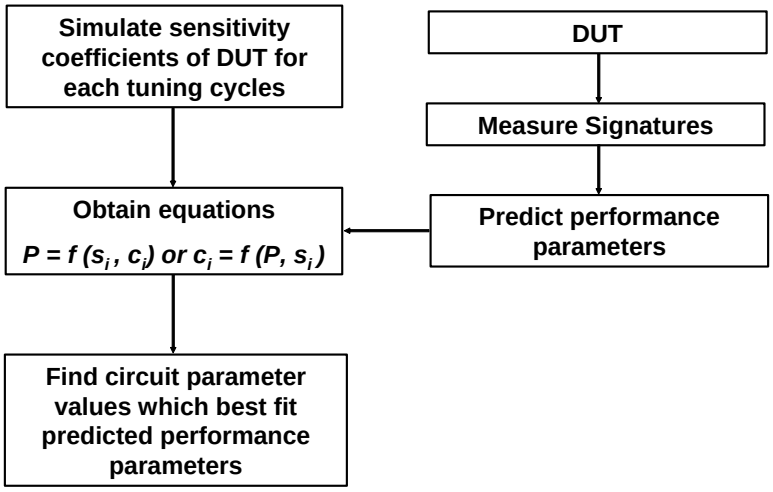


Figure 6.6: Implementation Flow of Fault Diagnosis using Parameter Tuning Technique

unknown variable.

6.4 Diagnosis Accuracy Improvement using Ensemble Method

In the scheme discussed in Section 6.2, the output measurement p_k is predicted from the signatures. The prediction errors caused by imperfect mapping functions or BIST circuitry, may cause significant errors in estimating the circuit parameters. Thus, Equation 6.13 can be re-written as follows.

$$\mathbf{P_U} = \dot{\mathbf{P}}_\mathbf{U} + \mathbf{S_U}\boldsymbol{\Gamma} + \boldsymbol{\Theta} + \mathbf{E} \tag{6.17}$$

where $\mathbf{E}$ is error matrix.

When we solve this nonlinear equations using nonlinear least square estimates, the error E can have a significant influence on the outcome. As

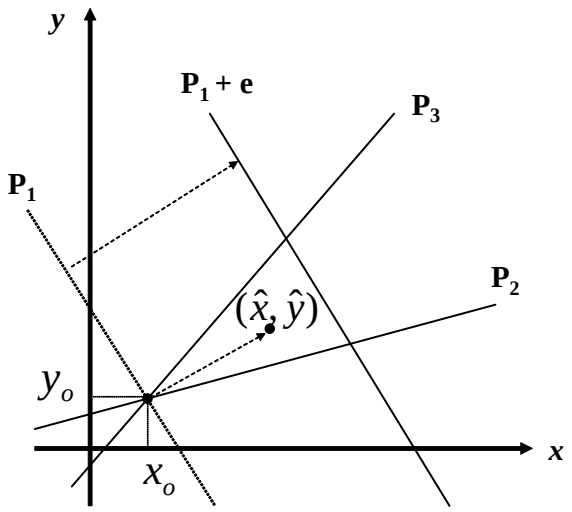


Figure 6.7: Erroneous Solution due to Measurement Error

all the equations contribute to find the optimal solutions, the optimal point may be shifted to fit the faulty equations, leading to the degradation of overall accuracy of the parameter estimation algorithm.

Consider an example shown in Figure 6.7 where circuit parameters x and y are predicted from three measured performance parameters p_i (i = 1, 2, 3) and linear functions $f_i(x, y)$ (i = 1, 2, 3) of variables x and y with sensitivity coefficients. If p_i and f_i are ideal, then the optimal estimates x_o and y_o would be the accurate solution. However, if p_1 is incorrectly predicted or measured with a significant error e induced by environmental noise or uncertainty in mapping functions, the estimates for variable x and y would be $\hat{x}$ and $\hat{y}$ which minimize

$$(p_1 + e - f_1(x, y))^2 + (p_2 - f_2(x, y))^2 + (p_3 - f_3(x, y))^2 \tag{6.18}$$

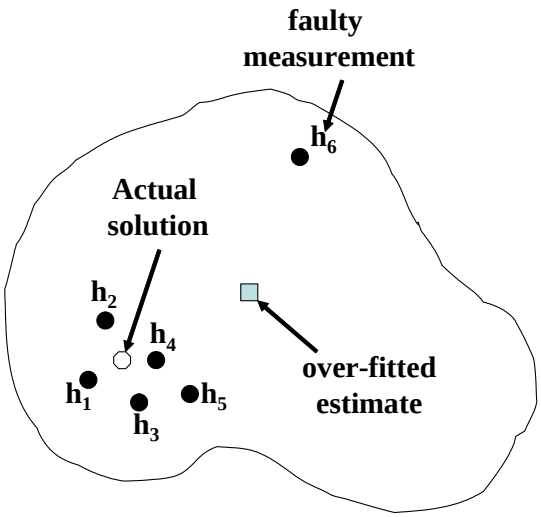


Figure 6.8: Example of Estimate Overfitting

Equation 6.18 indicates that a single error may dominate the estimation as the estimate is over-fitted to the error. In fact, the added complexity (increase of measurements) may lead to more serious over-fitting, because it is more likely that outliers like p_1 will appear. Figure 6.8 shows another example in which an outlier results in erroneous estimates.

In the following sections, an efficient diagnosis technique using an ensemble method which effectively handles large measurements obtained from parameter tuning and reduces over-fitting caused by measurement errors, is presented.

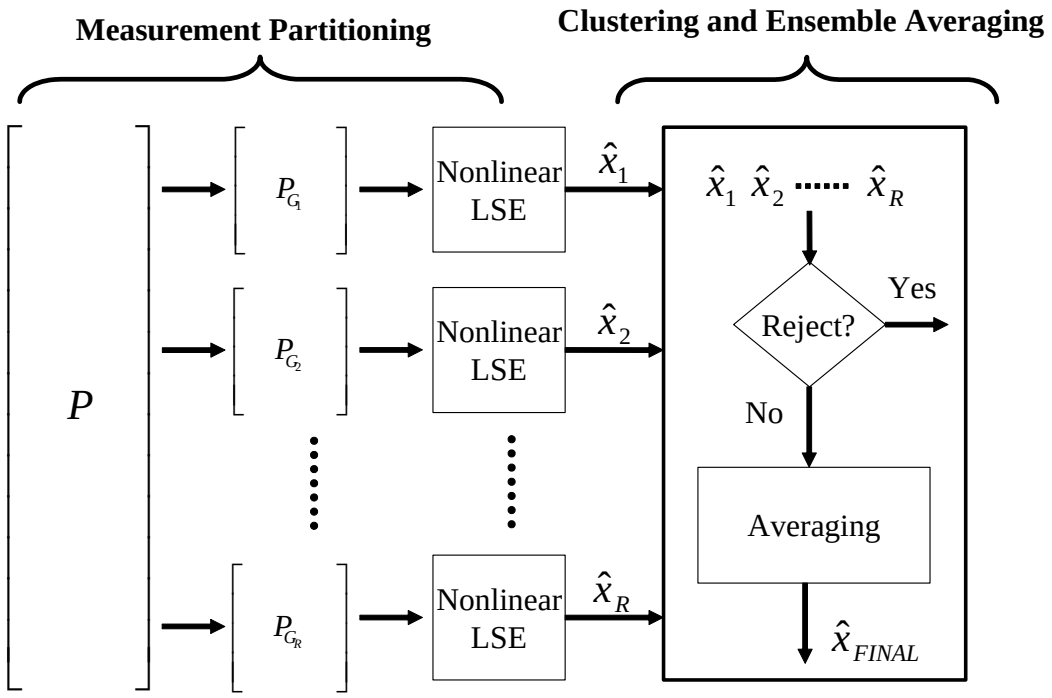


Figure 6.9: Ensemble Estimates

6.4.1 Ensemble Method

An ensemble method [39, 51] has been widely studied in the data mining and machine learning fields. The basic principle of an ensemble method is to develop a system in which the basic functionality is re-implemented with a number of models, and it pursues an effective combination of various models so as to compensate for each other's weaknesses, thus producing better decisions or predictions. An ensemble method is exploited to mitigate the faulty estimates due to over-fitting. Figure 6.9 shows the block diagram underlying the ensemble method. A measurement space which is diversified using parameter

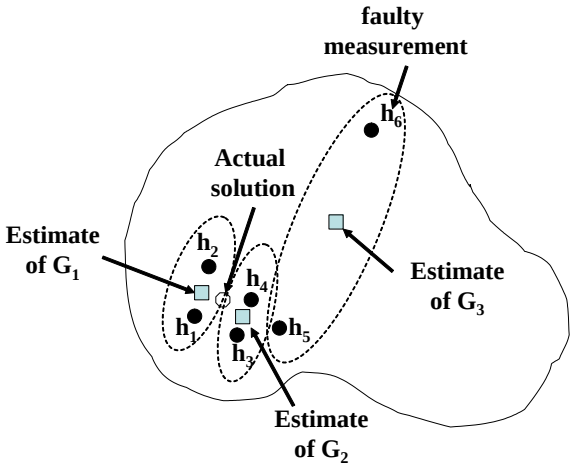


Figure 6.10: Estimate based on Ensemble Method

tuning is partitioned into groups of measurements. The groups of measurements are solved independently by a nonlinear equation solver. Then individual estimate $\hat{x_i}$ is evaluated by cross-correlations (distance) and uncorrelated estimates are pruned from the solution candidates. Finally, by averaging the remaining estimates, the final estimate is determined. For the example shown in Figure 6.8, the measurements is partitioned into three groups $G_1 = \{h_1, h_2\}$, $G_2 = \{h_3, h_4\}$ and $G_3 = \{h_5, h_6\}$ as shown in Figure 6.10. The estimates derived from G_1 and G_2 would be close to each other and the actual solution. However, the estimate from G_3 would be incorrect due to the error in the measurement h_6. The estimate is pruned from G_3, and use the remaining estimates from G_1 and G_2 are used to make the final estimate.

The following sections discuss the details of measurement partitioning and algorithm in order for the estimate rejection and ensemble averaging.

6.4.1.1 Measurement Partitioning

A condition for the ensemble estimate to be more accurate than any of its individual members, is that the partitioned measurements must be diverse. This condition prevents them making the same or similar mistakes [51]. However, this may contradict the diagnosability condition in which measurements and the corresponding sensitivity coefficients must be independent. Therefore, measurements must be carefully partitioned to balance these conditions. The use of testability analysis in solving non-linear equations has been well studied in [19]. The rank of the obtained Jacobian matrix of the LSE is used as a metric to measure the testability. The rank must be at least equal to the number of unknown circuit parameters.

6.4.1.2 Ensemble Estimates using K-means Clustering

Clustering algorithms are widely used in many different applications such as data compression, pattern recognition and pattern classification [52]. Among various clustering algorithms, K-means clustering is the most widely and commonly used algorithm employing a squared error criterion [34]. Given a set of n data points in real $\mathcal{D}$-dimensional space $\mathcal{R}^{\mathcal{D}}$ and an integer k, K-means clustering determines a set of k points in $\mathcal{R}^{\mathcal{D}}$, called centers, so as to minimize the mean squared distance from each data point to its nearest center [37]. K-means only has two input parameters: the number of clusters and the accuracy. For further information on clustering and K-means algorithm, see [34, 37, 52].

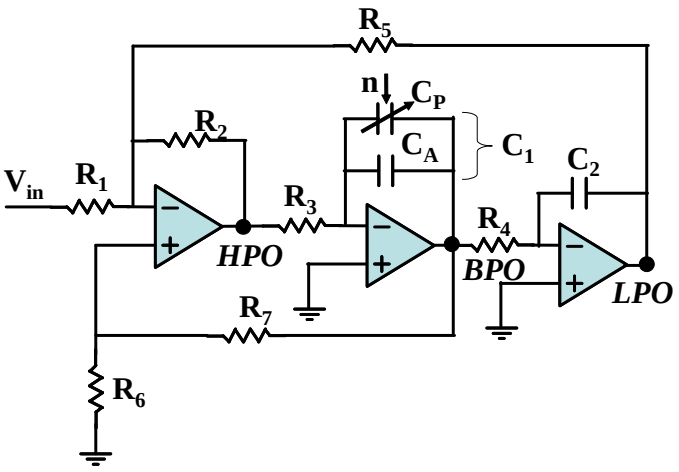


Figure 6.11: Tunable State-variable Benchmark Circuit

Three points (centers) in each circuit parameter space using K-means, are determined and then the center of the biggest cluster as the final estimate is chosen. For the case where more than one cluster has the same size as a majority, these clusters are merged, and the center of the merged cluster is re-calculated.

6.5 Simulation Results

A continuous-time state variable filter benchmark circuit [36] was re-designed with 3-bit PCA in the capacitor C_1 as shown in Figure 6.11. The reason that a PCA was employed rather than a resistor array is that the PCA is more frequently used as it has less impact on Signal-to-Noise Ratio (SNR), input impedance and system gain than programmable resistors. The value of C_u was 2.5% of the nominal value of C_1. Considering that a typical

Table 6.1: Diagnosed Parameters and Nominal Values

Parameters	R_2/R_1	R_5/R_1	R_7/R_6	C_1R_3	C_2R_4
Nominal Value	1	1	2.3	2e-4	2e-4

tuning circuitry in a practical implementation uses higher-bit PCA (7bits in [30]), 2.5% can be reasonable. The value of C_A was determined so that total capacitance of C_1 is equal to its nominal value when n is equal to 4. n is the digital code which controls the switches in the PCA.

Since the value of C_1 used in Figure 6.11 was too large, the value of C_u (0.5nF) may not be feasible in a real implementation of on-chip PCA. In addition, we may not see the parasitic effects induced by switch transistors (C_u is much bigger than the parasitic capacitance of the transistors). However, this value was used to compare our results with the previous work.

100 DUTs were generated by introducing statistical variations with an uniform distribution in values of circuit parameters ($R_1, \cdots, R_7$, C_1 and C_2) and C_u. It should be noted that the variation of C_u was not ignored; however, it was assumed the variation of matching of C_u ($2C_u$ and $4C_u$) is 1%.

By taking into account ambiguity fault classes [18], five parameters were considered, and Table 6.1 summarizes these fault classes and their nominal values. Among various methods to calculate sensitivities such as symbolic method, numerical and analytical method [27], a regression technique introduced in [18] was employed. The regression models were created to map the

circuit parameters to the selected performance parameters. The training data was generated through Hspice Monte-Carlo simulation. However, note that this method does not depend on the types of sensitivity calculation, and thus can be generally applied.

6.5.1 Second-order Sensitivity Effects of Tuning Parameters

Figure 6.12 shows the sensitivity of circuit parameters $(R_1, R_2, \cdots, R_7)$ with respect to four different specifications for various values of tuning parameter C_1. Here the sensitivities are normalized to 1. This result indicates that parameter tuning makes changes in circuit parameter's sensitivity. DC gain and Max gain increase almost linearly, but 3dB and phase show certain erratic responses. In fact, these erratic responses are more helpful in achieving uncorrelated output measurements.

6.5.2 Results using Parameter Tuning

In order to validate the effectiveness of diagnosability improvements obtained from the parameter tuning, the parameters in Table 6.1 were estimated using the measurements obtained from parameter tuning. Four performance parameters (gain, 3dB frequency, maximum gain and phase of lowpass output) were obtained from three tuning cycles. The obtained estimation results were then compared with the estimation using 11 specifications (4 parameters of each lowpass/highpass output and 3 parameters of bandpass output). In fact, it may not be possible to estimate five circuit parameter values only from

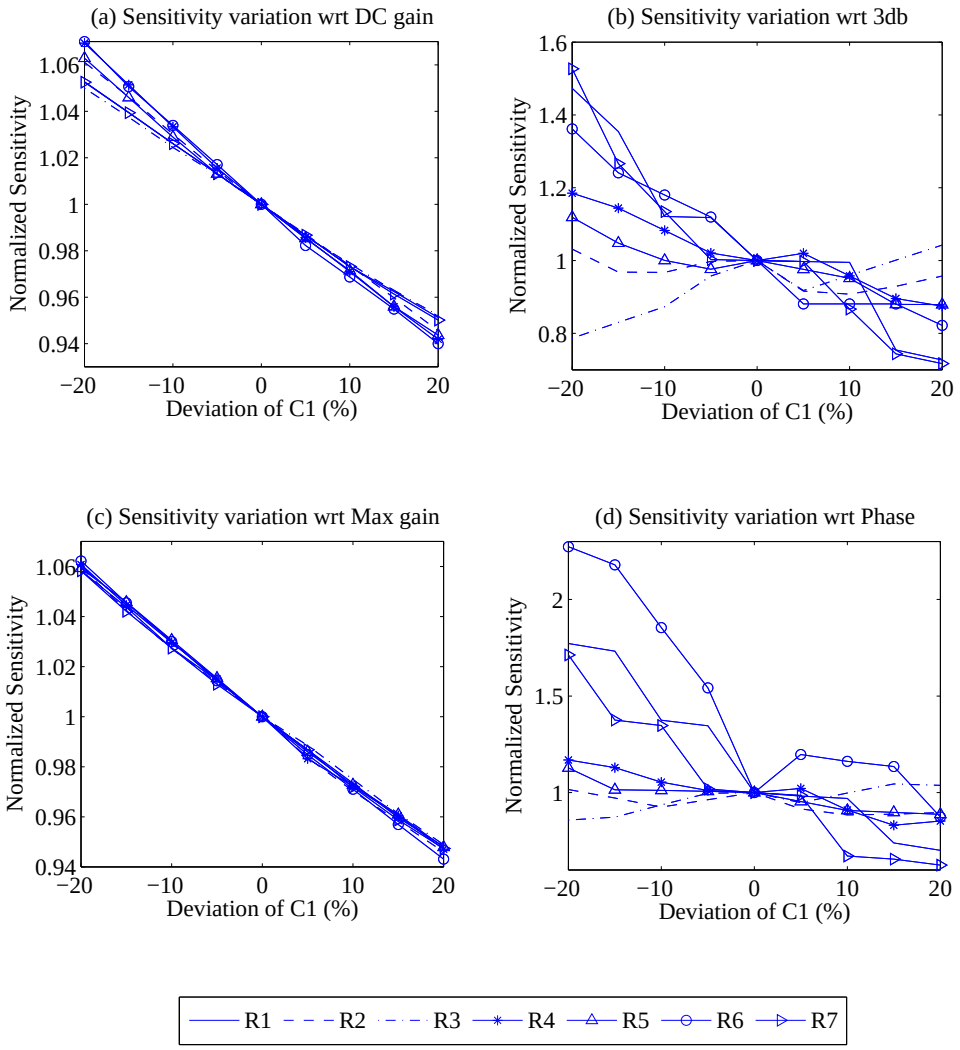
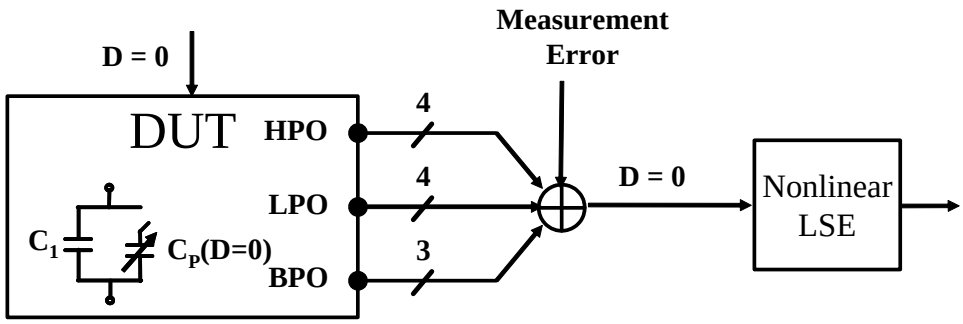
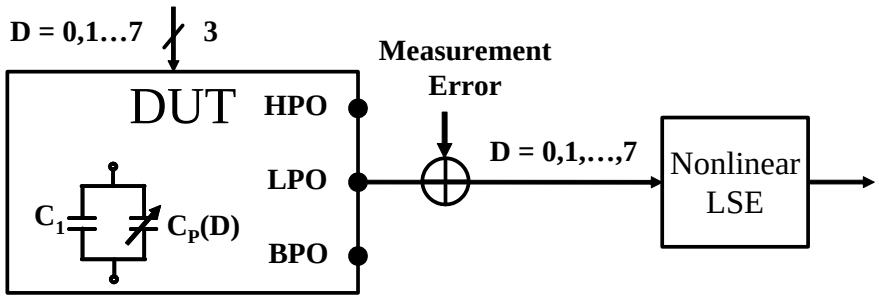


Figure 6.12: Sensitivity Variations for Tuning Parameter C_1



(a) Parameter Estimation based on 11 specifications and D = 0



(b) Parameter Estimation based on 4 specifications and D = 0,1,..7

Figure 6.13: Scheme for Fault Diagnosis using C_1 tuning (4 specifications)

four performance parameters without using the parameter tuning technique. There will be infinitely many solutions unless certain constraints or additional information are provided. Figure 6.13 shows the simulation set-ups for both approaches. The noise was injected into the measured performance parameters to emulate the measurement or prediction errors and noise in a real implementation. Table 6.2 shows that the estimation errors for the proposed method with 4 specifications and a method with 11 specifications. The estimation

Table 6.2: 11 Specifications versus 4 Specifications with Tuning

	Estimation Error (Mean for 100 DUTs)				
	R_2/R_1	R_5/R_1	R_7/R_6	C_1R_3	C_2R_4
11 specs.	1.6%	1.5%	2.7%	4.0%	3.8%
4 specs. with tuning	4.8%	1.5%	3.9%	3.7%	3.4%

errors were calculated based on the following equation.

$$\|Error\| = \frac{Actual \quad value - Predicted \quad value}{Actual \quad value} * 100 \tag{6.19}$$

Table 6.2 indicates that the method using the parameter tuning technique is as accurate as the method which uses much more measurements. Note that the ensemble method is not yet applied in this section.

6.5.3 Results using Ensemble Method

In this section, the fault diagnosis result using our ensemble method is presented. Figure 6.14 shows the estimation errors with respect to the number of tuning cycles. Here, 11 specifications were used for the estimation. The number in the x axis represents the number of tuning cycles used for the estimation (for example, 5 means tuning cycles from n = 2 to n = 6, and 0 means that tuning is not used). As can be seen in Figure 6.14, the estimation errors are decreased as more tuning cycles are used for the estimation.

Note that the value of C_u was also estimated. For 7 tuning cycles, the estimation errors was less than 1.5% except for C_u, and the estimation errors were reduced by more than 50% when they were compared with the case where

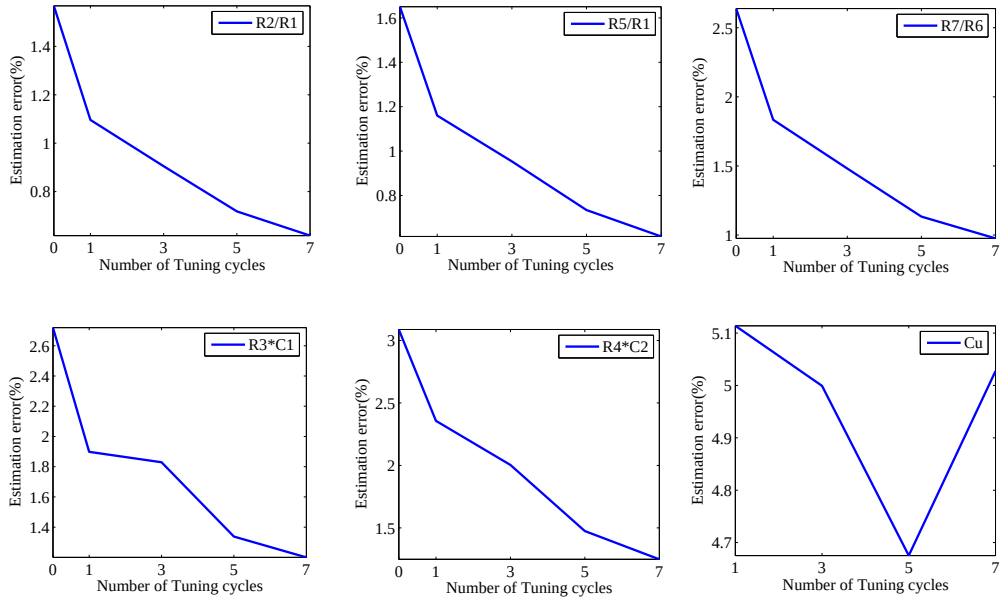


Figure 6.14: Estimation Error versus Total Number of Tuning Cycles

Table 6.3: Comparison with Previous Work

	Estimation Error (Mean)				
	R_2/R_1	R_5/R_1	R_7/R_6	C_1R_3	C_2R_4
Our method	0.7%	0.7%	1.1%	1.3%	1.1%
Previous method [18]	1.3%	1.3%	4.0%	2.5%	1.1%

no tuning cycles were used.

Also, the estimation errors of R_2/R_1 with respect to various measurement errors are shown in Figure 6.15. Unlike the proposed ensemble method which uses multiple LSEs, the single LSE approach used a single least square estimator on whole measurements obtained from the tuning. As shown in Figure 6.15, the ensemble method is less sensitive to measurement noise than a single LSE approach, and that by increasing the tuning cycles, more reliable results can be achieved.

6.5.4 Comparison with Previous Work

To the best of my knowledge, one other approach which discusses the estimation error rather than the detection error (determine whether circuit parameters are within tolerance limits) has been previously proposed in the literature [18]. This method uses the response of an additional internal node as well as the responses of primary outputs, and measurement errors are ignored in this method. Table 6.3 compares this previous method with the method presented in this chapter. In the ensemble method, 2% measurement error is additionally applied, but the previous method assumes ideal measurements. It

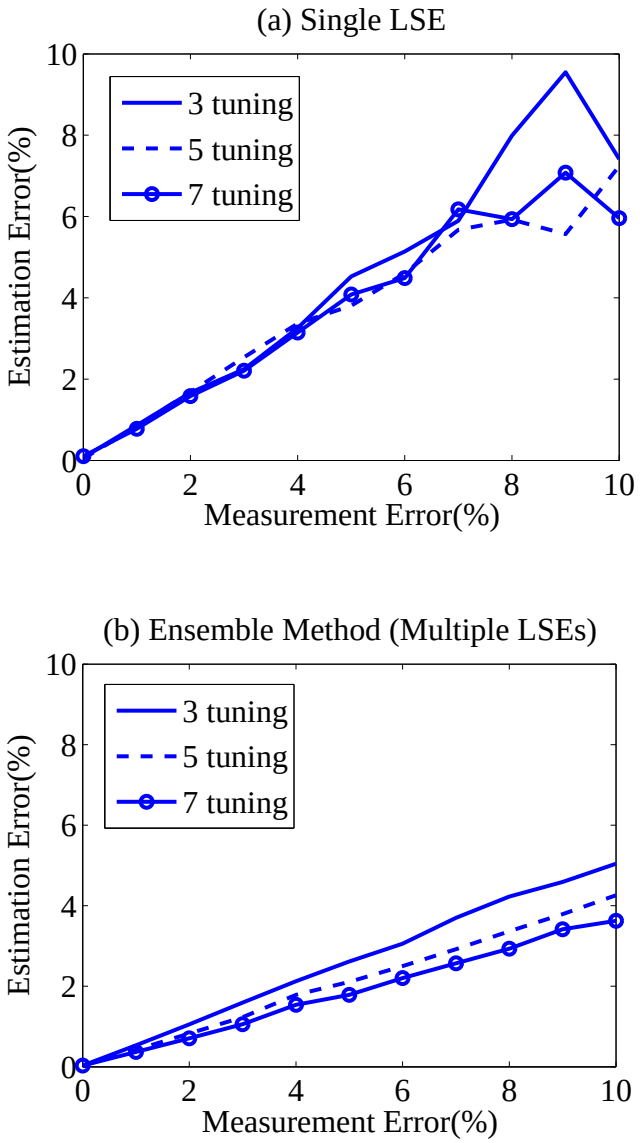


Figure 6.15: Estimation Error versus Injected Measurement Errors

can be seen that the proposed method still provides more accurate estimations.

6.6 Summary

A new low-cost fault diagnosis technique based on Built-in Self Test (BIST) was presented. The method enables rapid and accurate identification of weak spots in a design and potential problems in the manufacturing process, thereby leading to a significant reduction in time-to-market. Fault diagnosis is accelerated with available on-chip BIST which can generate low-cost signatures (performance parameters). Imperfect signatures due to limited on-chip resources and accuracy are compensated in two ways. Supplemental signatures are obtained from a re-configured Device Under Test (DUT) by parameter tuning, leading to improvements in diagnosability. Secondly, diagnosis accuracy is significantly improved by using an ensemble method which has been widely used in data mining. The technique can be used to identify single as well as multiple faults, and can also be used to facilitate a self-repair mechanism by accurately identifying the source of errors.

Chapter 7

Conclusion

The fundamental difficulty with analog testing is that it needs to handle a continuous signal with infinite precision. In addition, testing of deeply embedded analog and mixed-signal cores poses additional significant challenges. The aim of this thesis is to develop efficient self-test techniques to overcome such difficulties, focusing on the overall test cost reduction while maintaining the test accuracy equivalent to a traditional ATE-oriented test. This is achieved with several test techniques presented in this thesis. First, the considerable test cost associated with the measurement and excitation of analog signals motivates the Time-Encoded Signature (TES). There is some research on cost-effective on-chip implementation of a traditional test input generator [9, 46]; however, the adoption of this approach may be limited by the considerable design cost. Instead, the time encoded signature aims at simplified representation of analog signals, thereby achieving a significant cost reduction in analog signal measurement. Traditionally, the representation of analog signals is based on digitized amplitude information, which is usually achieved with elaborate Nyquist criteria. The time encoded signature is described with three levels, the rise time, the peak time and the slope. This is made possible with the fact that a simple analog signal is used during the test,

not an arbitrary analog signal which potentially includes many tones. The Time-Encoded Signature Decoder (TESD) was introduced to find the relation between the signature and the performance parameters, so that the performance of DUTs can be predicted with given signature values. The application limitations and potential source of errors of this method were discussed in this thesis. The resolution and speed of the comparator are important parameters which determines the test accuracy,and they pose tradeoffs between the test accuracy and the design cost.

A spectral prediction technique aims at attacking the fault masking problem, which has been a bottleneck in its wide application. A conventional loopback path is re-configured with the analog filter implemented on the DIB. A two-tone test input is applied to the DUT in this new loopback mode. The use of two tone is intended to achieve additional information from the loopback response. The filter on the DIB produces different weight for each tone, so that the ADC channel produces different responses according to the weights. Therefore, if the weights are known, then we can obtain sufficient information that the performance parameters of individual channel can be characterized. First, the characteristic equations which define the relation between the performance parameters and spectral parameters of the loopback response, are calculated. Then, the performance parameters which best fit the observed spectral parameters are obtained. Hardware measurement was performed on a commercial broadband IC. The results demonstrate that the performance of individual channels was successfully estimated with this technique. In this

thesis, the number of tones used is limited to two, but more tones can be used to improve the accuracy.

A statistical digital equalization technique was studied to overcome the precision limitation posed by DFT circuits, in particular, the DAC or the ADC in the loopback scheme for static linearity test. The transfer function of the DAC is estimated with the spectral prediction technique and Chebyshev polynomials. The digital equalizer is designed to compensate for the nonlinearity of the DAC in the pre-conversion stage, hence the ADC can be tested with the digitally calibrated analog signals. This result indicates that the performance limitation in DFT circuits or existing hardware which intend to replace ATE function can be overcome with proper digital processing without any additional analog measurements.

The aim of the analog fault diagnosis technique presented in this thesis is to provide collaborative methods with BIST and circuits for self-repair. As a consequence, the measurements, which traditionally use expensive external measurements of several test points, are replaced with signature measurements which can be achieved in a cost-effective way, and extra measurements which are needed for sufficient information are replaced with supplemental signatures generated by parameter tuning. Also, the ensemble method achieves a significant improvement in diagnosis accuracy by optimizing the fault identification procedure.

The self-test techniques discussed in this thesis, shows potentials in predicting the specifications of a mixed-signal system and its internal blocks

based on the re-use of existing digital and analog circuits. It is also shown that the obtained specifications can be employed for other testing purposes such as analog fault diagnosis and self-calibration. However, while the problems of analog fault diagnosis using self-test techniques were addressed in detail and overcome with the parameter tuning and the ensemble method, the application issues of self-test techniques combined with existing self-calibration algorithms still remains open problems. Since the reported self-calibration techniques is optimized under the assumption that the limited information is available, the fully characterized performance parameters may simplify the self-calibration algorithm, thereby reducing its hardware overhead.

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